

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

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PCN #: A1508-0	3 I	DATE: 11-Sep-2015	MEANS OF DISTI	NGUISHING CHA	NGED DEVICES:
Product Affected: Refer to A	6.0mm x 6.0mm VFQI ttachment II for the affe		□ Product Mark■ Back Mark□ Date Code□ Other	Lot # will have: "RC" prefix for A	ASECL, Taiwan
Date Effective: 1	1-Dec-2015				
Contact: ID	T PCN DESK		Attachment:	Yes	☐ No
E-mail: pc	ndesk@idt.com		Samples: Please co		les representative for
DESCRIPTION AN	D PURPOSE OF CHA	ANGE:			
 □ Die Technology □ Wafer Fabrication □ Assembly Process □ Equipment □ Material □ Testing ■ Manufacturing Sit □ Data Sheet □ Other 	This notification is to advise our customers that IDT is adding ASECL, Taiwan as the alternate Assembly facility. There is no change to the moisture performance. There is no change to the moisture performance. Attachment I details the qualification data for this change and Attachment II shows the affected list of part numbers.			ASECL, Taiwan as the	
	ALIFICATION SUM n data shown in Attachr				
CUSTOMER ACK	NOWLEDGMENT OF	F RECEIPT:			
to grant approval or it will be assumed th	that you require written request additional infor at this change is accept that to ship either version in has been depleted.	mation. If IDT does no able.	ot receive acknowledge	ement within 30 day	ys of this notice
Customer:			Approval for	shipments prior	r to effective date.
Name/Date:		I	E-Mail Address:		
Title:	Phone# /Fax# :				
CUSTOMER COM	MENTS:				
IDT ACKNOWI FI	OGMENT OF RECEI	рт			
			D.A.TE		
RECD. BY:			DATE:		

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ATTACHMENT I - PCN # : A1508-03

PCN Type: Manufacturing Site - Alternate Assembly Location

Data Sheet Change: None

No change in moisture sensitivity level (MSL)

Detail Of Change:

This notification is to advise our customers that IDT is adding ASECL, Taiwan as the alternate Assembly facility.

The material set details of the current and alternate assembly location is as shown in Table 1. The die attach and mold compound used at the alternate assembly are qualified IDT materials. There is no change from the existing qualified lead frame material and lead finish for the alternate assembly location.

There is no change to the moisture performance.

Table 1: Assembly Material Sets for The Existing and Alternate Assembly Location

	Existing Assembly (Amkor, Korea)	Alternate Assembly (ASECL, Taiwan)
Die Attach	CRM1085A	EN4900G
Wire	Au wire	PdCu wire
Mold Compound	G631BQF	G700LA

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ATTACHMENT I - PCN # : A1508-03

Qualification Information and Qualification Data:

Affected Packages: VFQFPN-36

Assembly Material: The affected package type is using ASECL standard materials shown on page 2

of this attachment.

Qual Plan & Results: Tests are in accordance with JEDEC47 recommended tests.

Qualification Vehicle: VFQFPN-32 (3 lots) with material sets as shown in page 2

		Test R	esults (S	S / Rej)
Test Description	Test Method	Lot 1	Lot 2	Lot 3
* HAST - biased (130 °C/85% RH, 96 Hrs)	JESD22-A110	25/0	25/0	25/0
* Temperature Cycle / Condition B (-55 °C to +125 °C, 700 Cyc)	JESD22-A104	25/0	25/0	25/0
High Temp. Storage Test (150 °C, 1000 Hrs)	JESD22-A103	25/0	25/0	25/0

Note:

^{*} Test requires moisture pre-conditioning sequence per JESD22-A113 prior to stress test

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ATTACHMENT II - PCN #: A1508-03

Affected Part Numbers

Part Number	Part Number	Part Number	Part Number
F1300NBGI	F1358NBGI	F1320NBGI8	F1375NBGI8
F1375NBGI	F1325NBGI8	F1320NBGI	
F1358NBGI8	F1325NBGI	F1300NBGI8	

		Current Site	Alternate Site
	Pkg and Si Attribute	Amkor Korea	ASECL Taiwan
	Pkg type	NBG36	NBG36
Pkg	Pkg x & y (mm)	6.0 mm x 6.0 mm	same
	Pkg z (mm)	0.8 mm	same
	Max Voltage	NA	NA
	Capacitors	NA	NA
	Si Process	No change	No change same wafer
	Wafer Size	No change	No change same wafer
	Die size (mm2)	No change	No change same wafer
	Die Aspect Ratio	No change	No change same wafer
	Die thickness (mils)	No change	No change same wafer
	Polyimide (Y/N)	No change	No change same wafer
	Silicon Metal Layers	No change	No change same wafer
	Scribe Width (um)	No change	No change same wafer
₽	UBM source	No change	No change same wafer
<u></u> ∞ŏ	Silicon UBM Stack-up	No change	No change same wafer
Silicon & FLI	Bump source	No change	No change same wafer
<u>:</u> 2	Bump pitch	No abanga	No change same wafer
Sil	I/O & Core (um)	No change	No change same water
	Total Bump count	No change	No change same wafer
	Bump Diameter	No change	No change same wafer
	Bump Height	No change	No change same wafer
	Bump Metallurgy	No change	No change same wafer
	Wafer Bump Flux	No change	No change same wafer
	CAM Flux	No change	No change same wafer
	Underfill Material	No change	No change same wafer
	Silicon UBM/SRO	No change	No change same wafer
	Halogen Free ?	NA	NA
	Substrate Layers	NA	NA
	Substrate thickness	NA	NA
	Core thickness (um)	NA	NA
	Core Material	NA	NA
	Outer layer Lines/space (um)	NA	NA
	Bump Pre-solder (SOP)	NA	NA
	Bump presolder (SOP)		
	height/diameter	NA	NA
	Bump Capture Pad/SRO IO	NA	NA
Φ	(um)	INA	INA
bstrate	Substrate Ball Capture Pad/SRO (um)	NA	NA
Sans	Number of PTH/M1-M2	NA	NA
0)	uVias Core PTH/Capture pad	IVA	IVA
	(um)	NA	NA
	Substrate Design Rule & BOM	NA	NA
	Substrate Supplier	NA	NA
	Build up layer (thickness)	NA	NA
	Solder mask (thickness)	NA	NA
	C1 & C4 thickness (plate)	NA	NA
	C2 & C3 thickness (foil +	NA	NA
	plate) Surface finish (thickness)	NA	NA NA
	2nd level Ball count	NA NA	NA NA
	2nd level BA Flux	NA NA	NA NA
SLI	2nd Ball Dia (mm)	NA	NA NA
S	2nd level metallurgy	NA NA	NA NA
	2nd level ball pitch (mm)	NA NA	NA NA
		- ** *	