

General Description

The ICS844011 is a Fibre Channel Clock Generator. The ICS844011 uses an 18pF parallel resonant crystal. For Fibre Channel applications, a 26.5625MHz crystal is used. The ICS844011 has excellent <1ps phase jitter performance, over the 637kHz - 10MHz integration range. The ICS844011 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

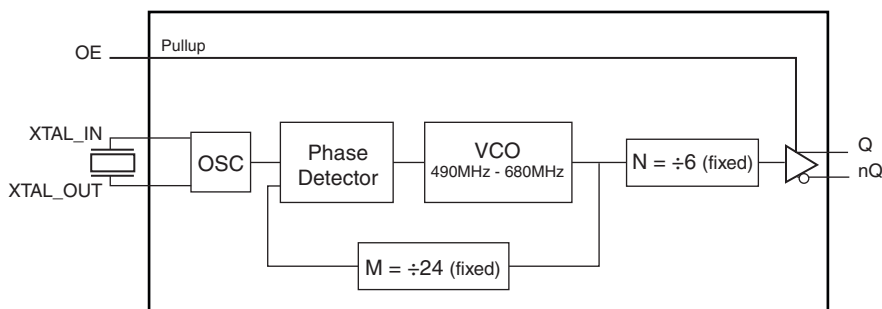
Features

- One differential LVDS clock output pair
- Crystal interface designed for 18pF parallel resonant crystals
- VCO range: 490MHz – 680MHz
- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.97ps (typical)
- RMS phase jitter @ 100MHz, (637kHz - 10MHz): 0.77ps (typical)
- Full 3.3V or 2.5V operating supply
- Available in lead-free (RoHS 6) package
- 0°C to 70°C ambient operating temperature

Common Configuration Table – Fibre Channel

Inputs				Output Frequency (MHz)
Crystal Frequency (MHz)	M	N	Multiplication Value M/N	
26.5625	24	6	4	106.25
25	24	6	4	100

Block Diagram



Pin Assignment

VDDA	1	8	VDD
GND	2	7	Q
XTAL_OUT	3	6	nQ
XTAL_IN	4	5	OE

ICS844011
8-lead TSSOP
4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V _{DDA}	Power		Analog power supply.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Output enable pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock output. LVDS interface levels.
8	V _{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3. OE Control Function Table

Input	
OE	Output Enable
0	Output Q, nQ pair is disabled in high-impedance state.
1 (default)	Output Q, nQ is enabled.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Input	0V to V_{DD} -0.5V to $V_{DD} + 0.5V$
Outputs, I_O Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.12$	3.3	V_{DD}	V
I_{DD}	Power Supply Current				108	mA
I_{DDA}	Analog Supply Current				12	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.12$	2.5	V_{DD}	V
I_{DD}	Power Supply Current				102	mA
I_{DDA}	Analog Supply Current				12	mA

Table 4C. LVCMOS/LVTTL Input DC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	OE $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	μA
I_{IL}	Input Low Current	OE $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			μA

Table 4D. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.1	1.3	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4E. LVDS DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		0.9	1.2	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		25		26.5625	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Characteristics

Table 6A. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		100		106.25	MHz
$\text{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	106.25MHz, Integration Range: 637kHz – 10MHz		0.97		ps
		100MHz, Integration Range: 637kHz – 10MHz		0.77		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		400	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

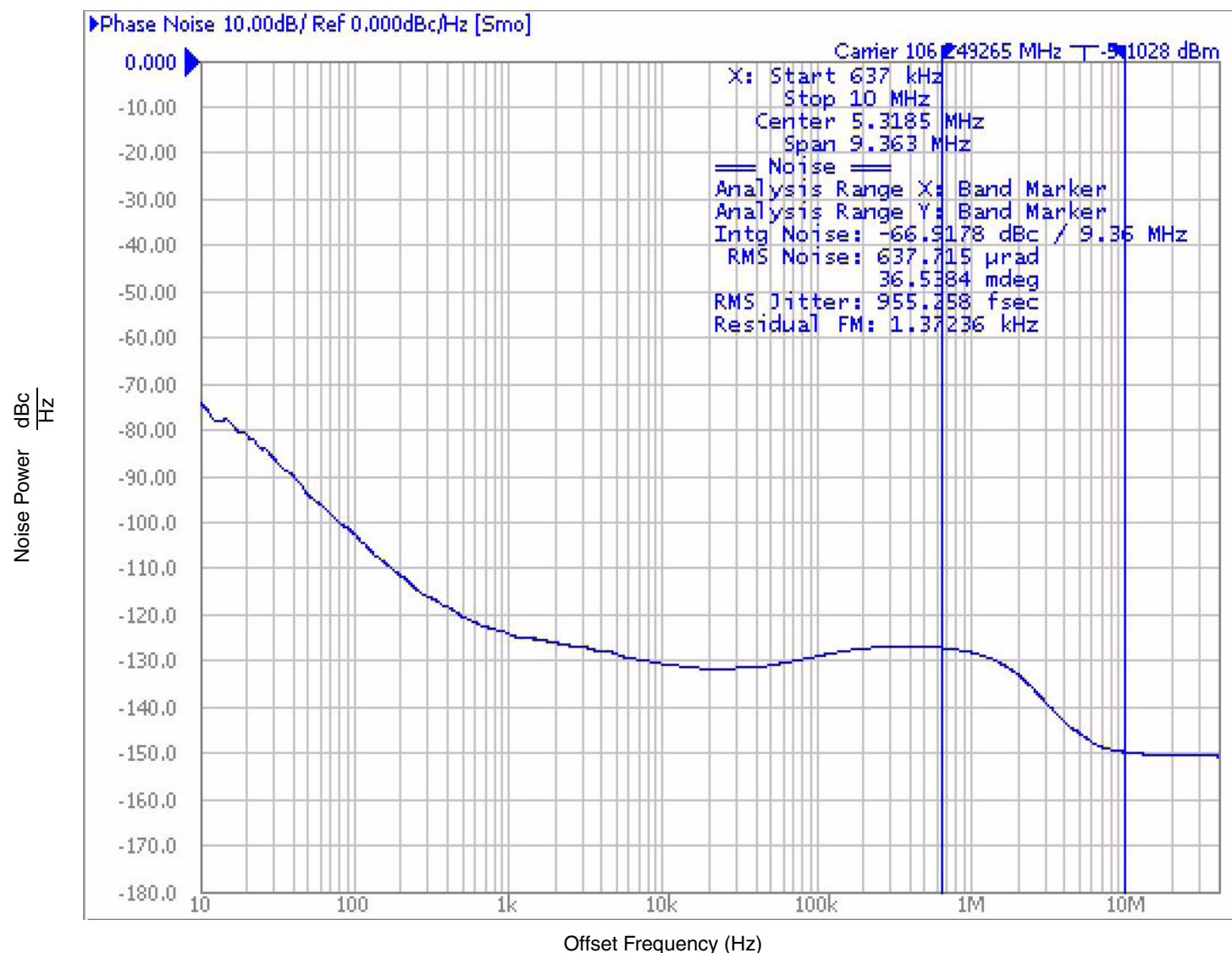
NOTE 1: Please refer to the phase noise plot.

Table 6B. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

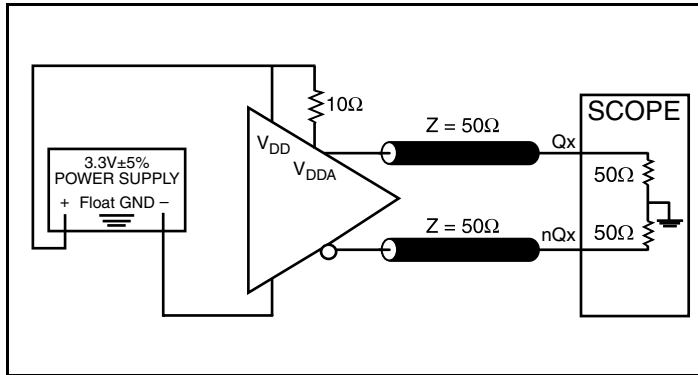
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		100		106.25	MHz
$\text{jit}(\emptyset)$	RMS Phase Jitter (Random)	106.25MHz, Integration Range: 637kHz – 10MHz		1.26		ps
		100MHz, Integration Range: 637kHz – 10MHz		0.98		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		400	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

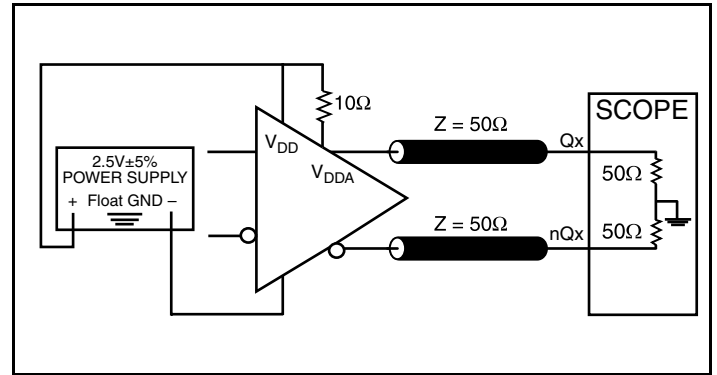
Typical Phase Noise at 106.25MHz (3.3V)



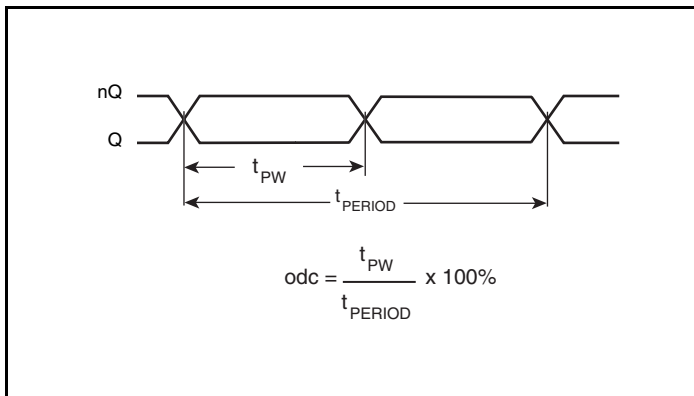
Parameter Measurement Information



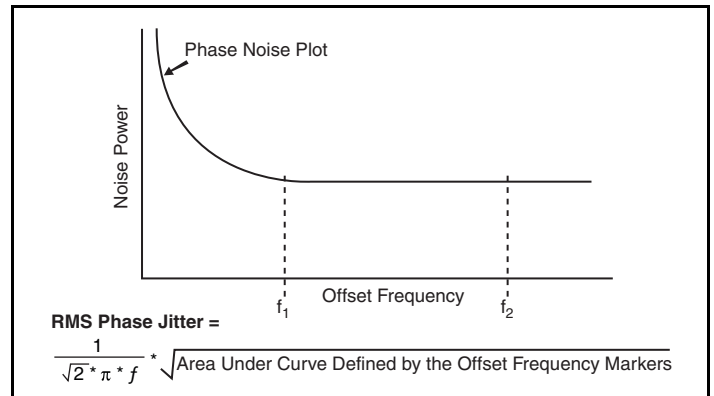
3.3V LVDS Output Load Test Circuit



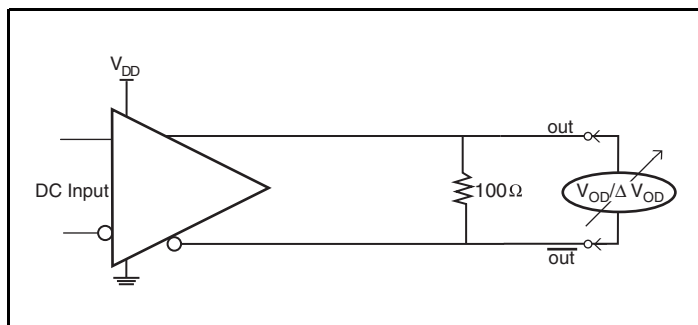
2.5V LVDS Output Load Test Circuit



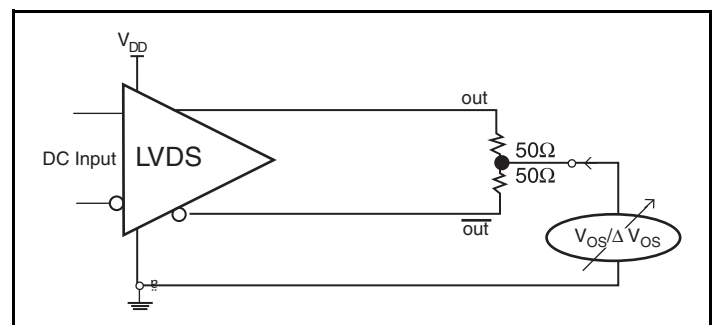
Output Duty Cycle/Pulse Width/Period



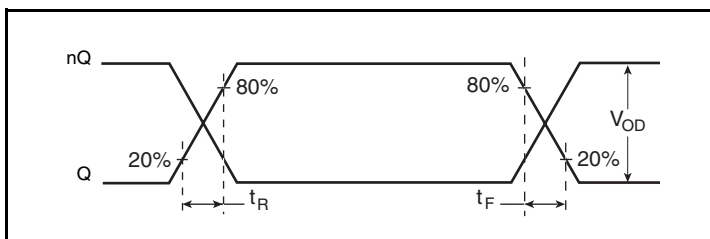
RMS Phase Jitter



Differential Output Voltage Setup



Offset Voltage Setup



Output Rise/Fall Time

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and changing R_2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

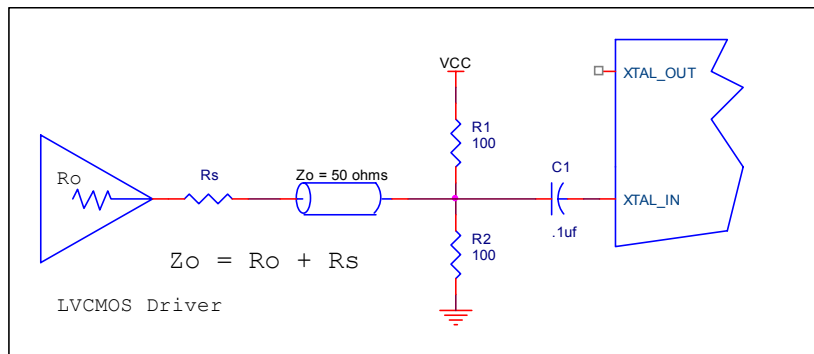


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

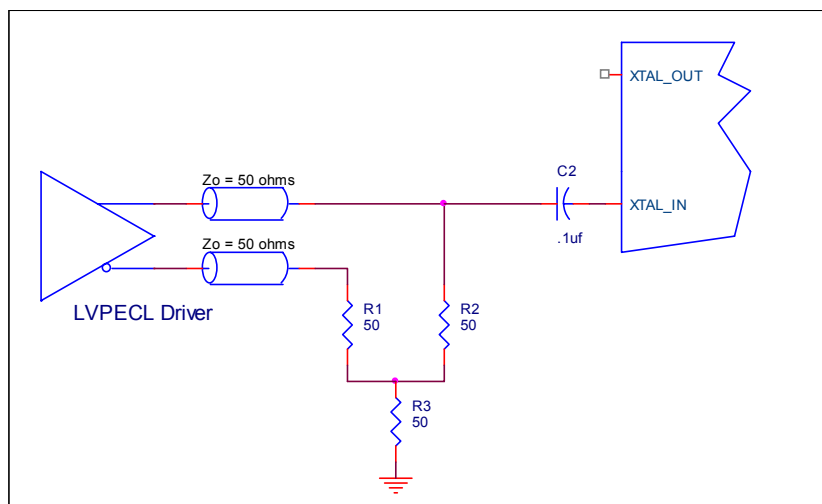
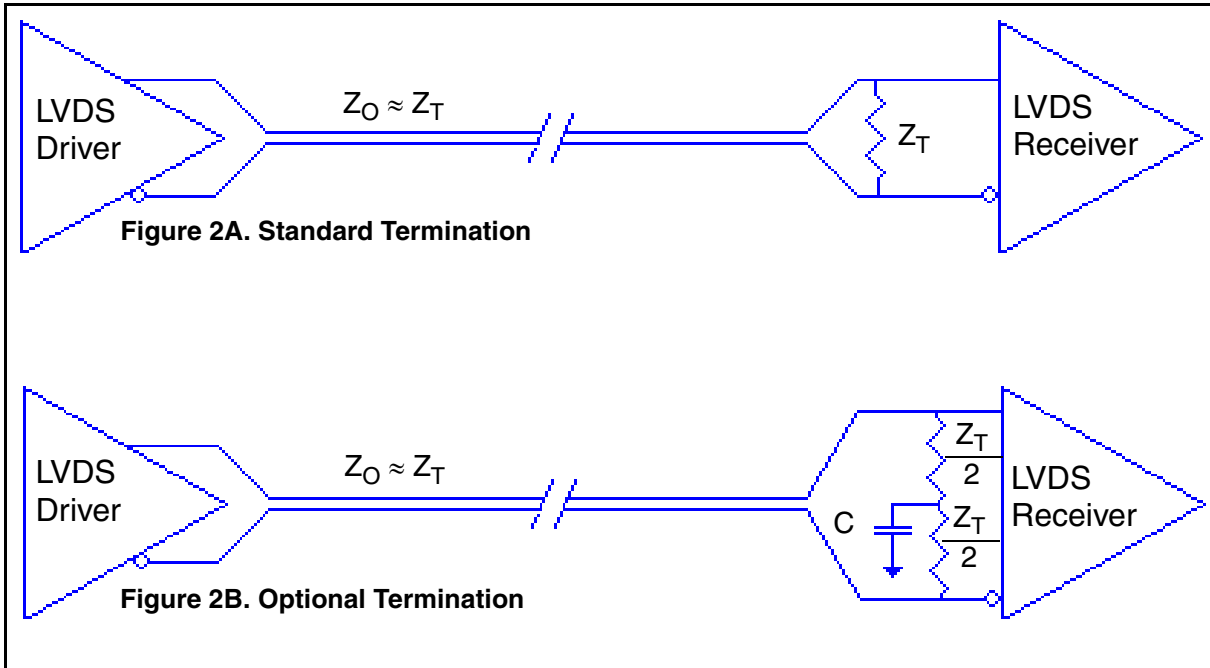


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

Schematic Layout

Figure 3 shows an example of ICS844011 application schematic in which the device is operated at $V_{DD} = 3.3V$. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example OE can be configured from an FPGA instead of set with pull up and pull down resistors as shown.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{DD} pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB

as close to the power pins as possible. If space is limited, the 0.1uF capacitor on the VDD pin must be placed on the device side with direct return to the ground plane through vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

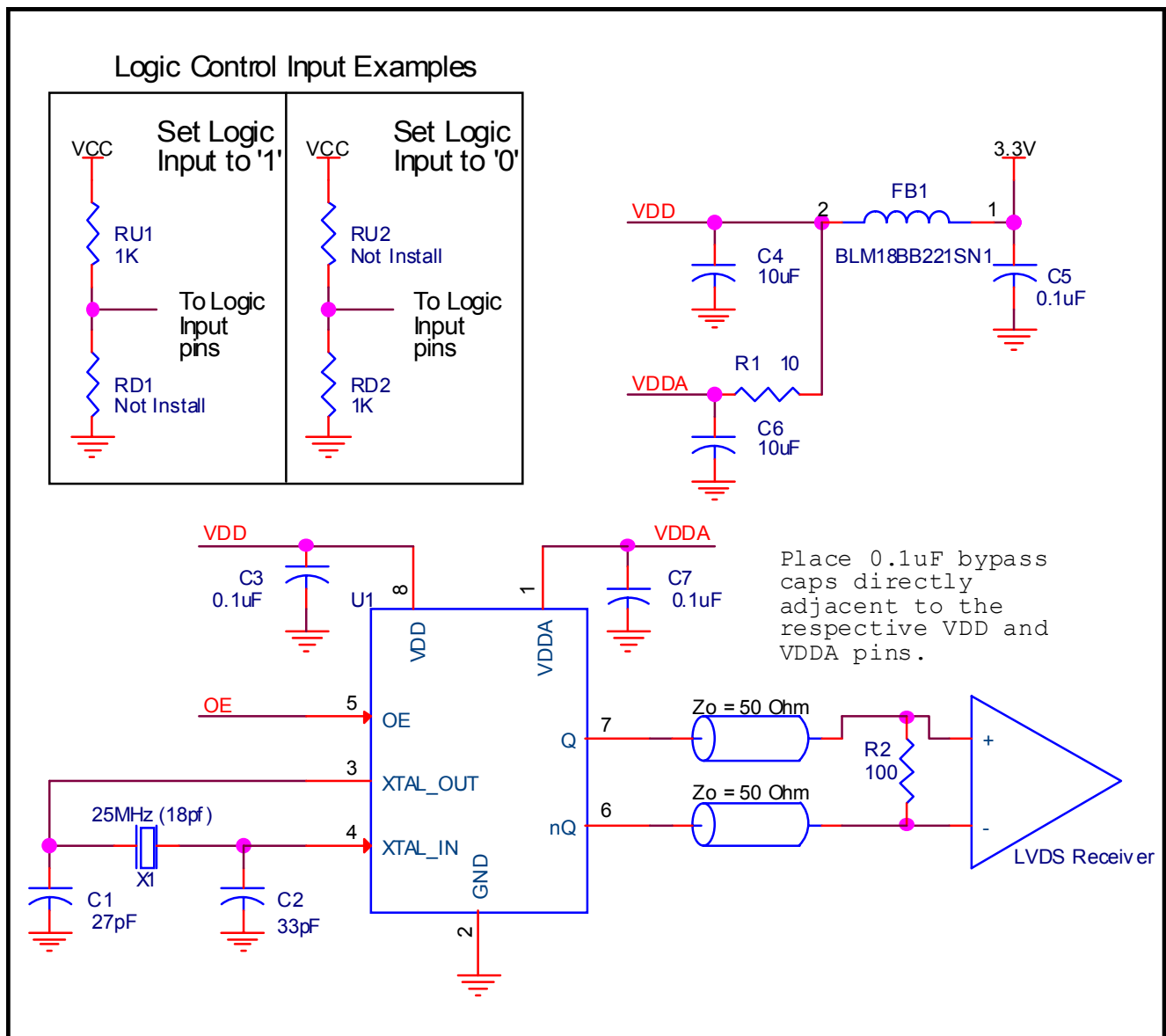


Figure 3. ICS844011 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844011. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844011 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (108mA + 12mA) = \mathbf{415.8mW}$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^{\circ}C + 0.416W * 129.5^{\circ}C/W = 123.9^{\circ}C. \text{ This is below the limit of } 125^{\circ}C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 8-lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Transistor Count

The transistor count for ICS844011 is: 2533

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

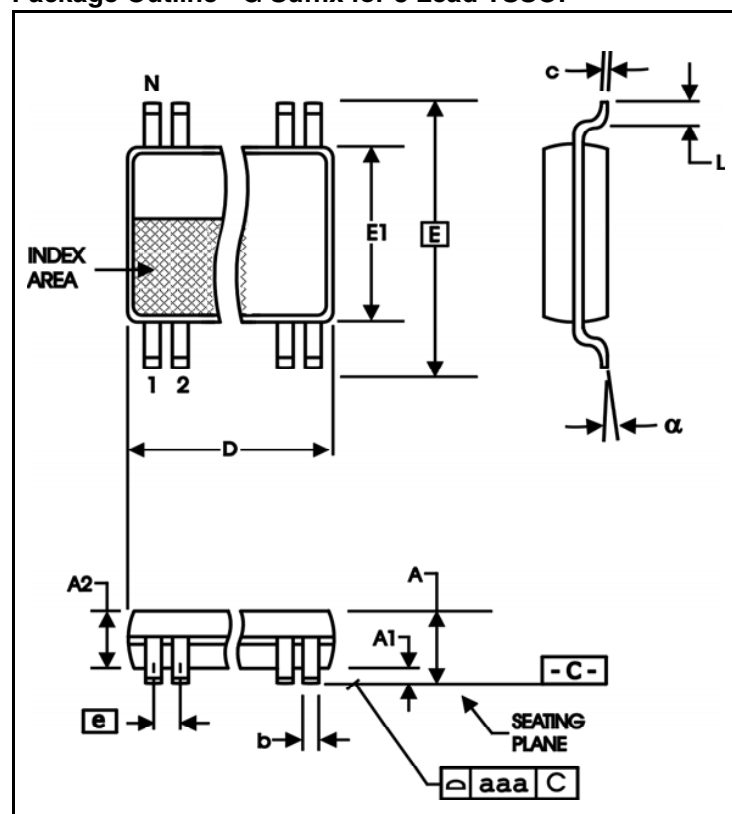


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844011AGLF	011AL	Lead-Free, 8-lead TSSOP	Tube	0°C to 70°C
844011AGLFT	011AL	Lead-Free, 8-lead TSSOP	Tape & Reel	0°C to 70°C

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