

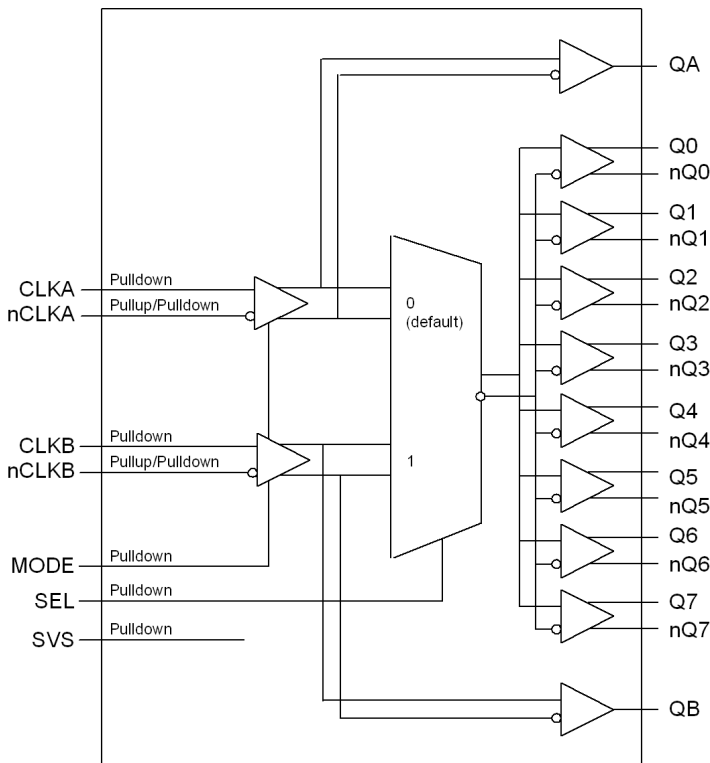
### General Description

The 8V34S208 is a differential 1:8 LVDS fanout buffer with a 2:1 input multiplexer. The device accepts DC to 250MHz clock and data signals and is designed for 1Hz clock /1PPS, 2kHz and 8kHz signal distribution. Controlled by the input mode selection pin, the differential input stages accept both rectangular or sinusoidal signals. The 8V34S208 also provides level translated LVCMOS/LVTTL outputs which are copies of the individual differential inputs CLKA and CLKB. The propagation delay of the device is very low, providing an ideal solution for clock distribution circuits with tight phase alignment requirements. The multiplexer select pin (SEL) allows to select one out of two input signals, which is copied to the four differential outputs.

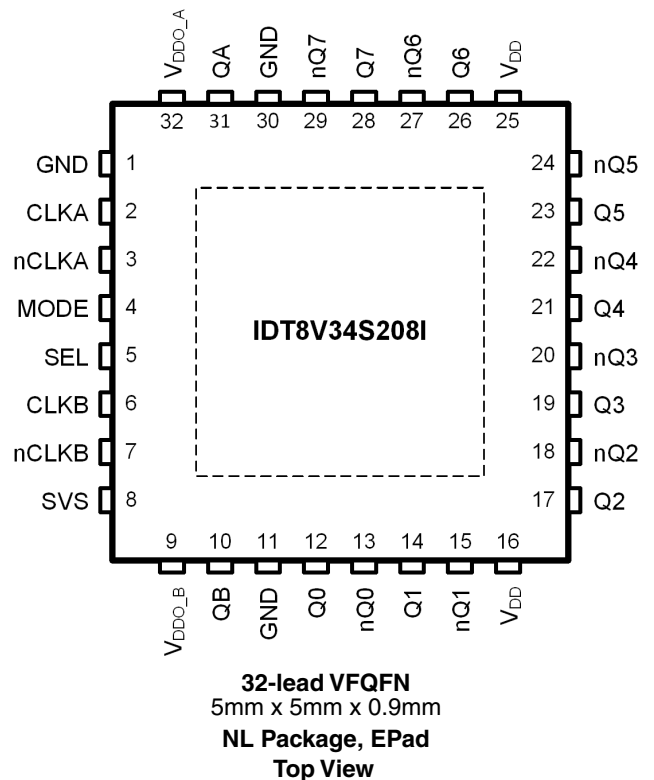
### Features

- Designed for 1PPS, 2kHz, 8kHz and 10MHz GPS clock signal distribution
- High speed 1:8 LVDS fanout buffer
- Eight differential LVDS output pairs
- 2:1 input multiplexer
- Two selectable differential inputs accept LVDS and LVPECL signals
- Accepts rectangular and sinusoidal input signals
- Two input monitoring outputs (LVCMOS)
- Max output frequency: 250 MHz
- Additive RMS phase jitter: 118fs (typical) at 100MHz (12k-20Mhz)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 325ps (typical), LVDS output
- Full 2.5V and 3.3V voltage supply
- -40°C to 85°C ambient operating temperature
- Lead-free 32-lead VFQFN (RoHS 6/6) packaging

### Block Diagram



### Pin Assignment



## Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	GND	Power		Power supply ground.
2	CLKA	Input	Pulldown	Non-inverting differential clock input.
3	nCLKA	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
4	MODE	Input	Pulldown	Input mode pin. See Table 3B. LVCMOS/LVTTL interface levels.
5	SEL	Input	Pulldown	Input selection pin. See Table 3A. LVCMOS/LVTTL interface levels.
6	CLKB	Input	Pulldown	Non-inverting differential clock input.
7	nCLKB	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
8	SVS	Input	Pulldown	Supply Voltage Select. See Table 3C. LVCMOS/LVTTL interface levels.
9	$V_{DDO\_B}$	Power		Output supply pin for QB output.
10	QB	Output		Single-ended QB clock output. LVCMOS/LVTTL interface levels.
11	GND	Power		Power supply ground.
12	Q0	Output		Differential output pair. LVDS interface levels.
13	nQ0	Output		
14	Q1	Output		Differential output pair. LVDS interface levels.
15	nQ1	Output		
16	$V_{DD}$	Power		Power supply pins for the device core
17	Q2	Output		Differential output pair. LVDS interface levels.
18	nQ2	Output		
19	Q3	Output		Differential output pair. LVDS interface levels.
20	nQ3	Output		
21	Q4	Output		Differential output pair. LVDS interface levels.
22	nQ4	Output		
23	Q5	Output		Differential output pair. LVDS interface levels.
24	nQ5	Output		
25	$V_{DD}$	Power		Power supply pins for the device core
26	Q6	Output		Differential output pair. LVDS interface levels.
27	nQ6	Output		
28	Q7	Output		Differential output pair. LVDS interface levels.
29	nQ7	Output		
30	GND	Power		Power supply ground.
31	QA	Output		Single-ended QA clock output. LVCMOS/LVTTL interface levels.
32	$V_{DDO\_A}$	Power		Output supply pin for QA output.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance	MODE, SEL, SVS		2		pF
$R_{PULLDOWN}$	Pulldown Resistor			50		k $\Omega$
$R_{PULLUP}$	Pullup Resistor			50		k $\Omega$
$C_{PD}$	Power Dissipation Capacitance (per output)	$V_{DD}, V_{DDO\_A}, V_{DDO\_B} = 3.465V$		6		pF
		$V_{DD}, V_{DDO\_A}, V_{DDO\_B} = 2.625V$		6		pF
$R_{OUT}$	Output Impedance	QA, QB $V_{DDO\_A}, V_{DDO\_B} = 3.3V \pm 5\%$		27		$\Omega$
		QA, QB $V_{DDO\_A}, V_{DDO\_B} = 2.5V \pm 5\%$		30		$\Omega$

## Function Tables

**Table 3A. Input Selection Function Table**

Input	Outputs		
SEL	Q[0:7], nQ[0:7]	QA	QB
0 (default)	CLKA	CLKA	CLKB
1	CLKB	CLKA	CLKB

**Table 3B. Input Mode Function Table<sup>1</sup>**

Input	Operation
MODE	CLKA, CLKB
0 (default)	Inputs accept rectangular signals
1	Inputs accept sinusoidal signals

NOTE 1: Use a rectangular wave input for inputs with edge rate greater than 1V/ns.

**Table 3C. Supply Voltage Select Function Table**

Input	Operation
SVS	Supply Voltage
0 (default)	Set to logic 0 when $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 2.5V$
1	Set to logic 1 when $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V$

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ (LVCMOS)	-0.5V to $V_{DDO\_X} + 0.5V$
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	10mA 15mA
Maximum Junction Temperature, $T_{J, MAX}$	125°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
ESD - Human Body Model <sup>1</sup>	2000V
ESD - Charged Device Model <sup>1</sup>	1500V

NOTE 1: According to JEDEC/JESD 22-A114/22-C101.

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO\_A}$ , $V_{DDO\_B}$	LVCMOS Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current			158	184	mA
$I_{DDO\_A} +$ $I_{DDO\_B}$	LVCMOS Output Supply Current	Outputs Unterminated		6	8	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO\_A}$ , $V_{DDO\_B}$	LVCMOS Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current			150	174	mA
$I_{DDO\_A} +$ $I_{DDO\_B}$	LVCMOS Output Supply Current	Outputs Unterminated		5	8	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage			2.2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage			-0.3		0.8	V
$I_{IH}$	Input High Current	SEL, MODE, SVS	$V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	SEL, MODE, SVS	$V_{DD} = 3.465V, V_{IN} = 0V$	-10			$\mu A$
$V_{OH}$	Output High Voltage	QA, QB	$I_{OH} = -8mA$	2.6			V
$V_{OL}$	Output Low Voltage	QA, QB	$I_{OL} = 8mA$			0.5	V

**Table 4D. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage			1.8		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage			-0.3		0.6	V
$I_{IH}$	Input High Current	SEL, MODE, SVS	$V_{DD} = V_{IN} = 2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	SEL, MODE, SVS	$V_{DD} = 2.625V, V_{IN} = 0V$	-10			$\mu A$
$V_{OH}$	Output High Voltage	QA, QB	$I_{OH} = -8mA$	1.8			V
$V_{OL}$	Output Low Voltage	QA, QB	$I_{OL} = 8mA$			0.5	V

**Table 4E. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLKA, CLKB, nCLKA, nCLKB	$V_{DD} = V_{IN} = V_{DDMAX}$			150	$\mu A$
$I_{IL}$	Input Low Current	CLKA, CLKB	$V_{DD} = V_{DDMAX}, V_{IN} = 0V$	-10			$\mu A$
		nCLKA, nCLKB	$V_{DD} = V_{DDMAX}, V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Voltage <sup>1</sup>			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage <sup>1, 2</sup>			1		$V_{DD} - (V_{PP}/2)$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V and  $V_{IH}$  should not be higher than  $V_{DD}$ .

NOTE 2: Common mode input voltage is defined at the crosspoint.

**Table 4F. LVDS Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage			247	390	454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change					50	mV
$V_{OS}$	Offset Voltage			1.05	1.2	1.375	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change					50	mV

**Table 4G. LVDS Differential DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		247	373	454	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.05	1.2	1.375	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ <sup>1</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency				250	MHz
$\Delta V/\Delta t$	Input Edge Rate <sup>2</sup>	CLKA, CLKB MODE = 0	1			V/ns
$t_{PD}$	Propagation Delay <sup>3</sup>	CLKA, CLKB to Q[0-3], nQ[0-3]	200	325	434	ps
	Propagation Delay <sup>4</sup>	CLKA, CLKB to QA, QB	970	1.20	1.62	ns
$f_{jit}(\emptyset)$	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	Q[0-3], nQ[0-3] $f_{OUT} = 156.25\text{MHz}$ , Integration Range: 12kHz – 20MHz, MODE 0		118	170	fs
$tsk(pp)$	Part-to-Part Skew <sup>5 6</sup>	Q[0-3], nQ[0-3]			250	ps
$tsk(o)$	Output Skew <sup>6</sup>	Q[0-3], nQ[0-3] <sup>7</sup>			65	ps
		QA-QB <sup>8</sup>			65	ps
		All outputs			1.3	ns
$tsk(p)$	Pulse Skew <sup>9, 10</sup>	Q[0-3], nQ[0-3]		11	62	ps
		QA, QB		75	140	ps
$t_R / t_F$	Output Rise/ Fall Time	QA, QB; 20% to 80%		200	350	ps
		Q[0-3], nQ[0-3] 20% to 80%		125	250	ps
$MUX_{ISOLATION}$	MUX Isolation <sup>11</sup>	$f_{OUT} = 100.00\text{MHz}$ , $V_{PP} = 400\text{mV}$		53		dB

NOTE 1: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2: In MODE = 1 sinusoidal input signals are permitted and no minimum input edge rate specification applies.

NOTE 3: Measured from the differential input crosspoint to the differential output crosspoint using an input with 50% duty cycle.

NOTE 4: Measured from the differential input crosspoint to the output at  $V_{DDO\_X/2}$  using an input with 50% duty cycle.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 7: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

NOTE 8: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO\_X/2}$  of the output.

NOTE 9: Output pulse skew  $t_{SK(P)}$  is the absolute difference of the propagation delay times:  $|t_{PLH} - t_{PHL}|$ .

NOTE 10:  $odc = \text{input duty cycle} \pm (t_{SK(P)}/2 * 1/\text{Output Period}) * 100$

NOTE 11: Qx, nQx output measured differentially. See Parameter Measurement Information for MUX Isolation diagram.

**Table 6. Characteristics for 1PPS operation,  $V_{DD} = 3.3V \pm 5\%$  or  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ <sup>1 2 3 4</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
T	Input and Output Pulse Period			1		s
$T_P$	Positive or Negative Pulse Width		100			ns
$t_{PD}$	Propagation Delay;	CLKx/nCLKx to Qx/nQx		300	650	ps
$tsk(p)$	Pulse Width Distortion	CLKx/nCLKx to Qx/nQx		55	300	ps
$tsk(o)$	Output Skew <sup>5</sup>	Qx/nQx to Qy/nQy			325	ps
$tsk(pp)$	Part-to-Part Skew <sup>6</sup>				350	ps
$t_R / t_F$	Output Rise/Fall Time	10% to 90%	50	150	350	ps

NOTE 1: 1PPS (one pulse per second) signals are defined as repetitive pulses with a rate (period) of 1Hz. The positive input pulse width may vary. The active signal edge is the rising edge. Parameters in this table are characterized for a positive input pulse width of 100ns, 100ms and 500ms; All device interfaces are DC-coupled. Parameters are defined in accordance with ITU-T G.703 Amendment 1 - Specifications for the physical layer of the ITU-T G8271/Y.1366 time synchronization interfaces.

NOTE 2: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 3:  $t_{PD}$ ,  $t_{SK(O)}$ ,  $t_{SK(P)}$  and  $t_{SK(P)}$  parameters of differential signals are referenced to the crosspoint.

NOTE 4: Differential outputs for 1PPS signal transmission are terminated balanced 100 $\Omega$  according to the LVDS Output Load Test Circuit figures. The dedicated 1PPS outputs are the differential outputs Q0-Q3.

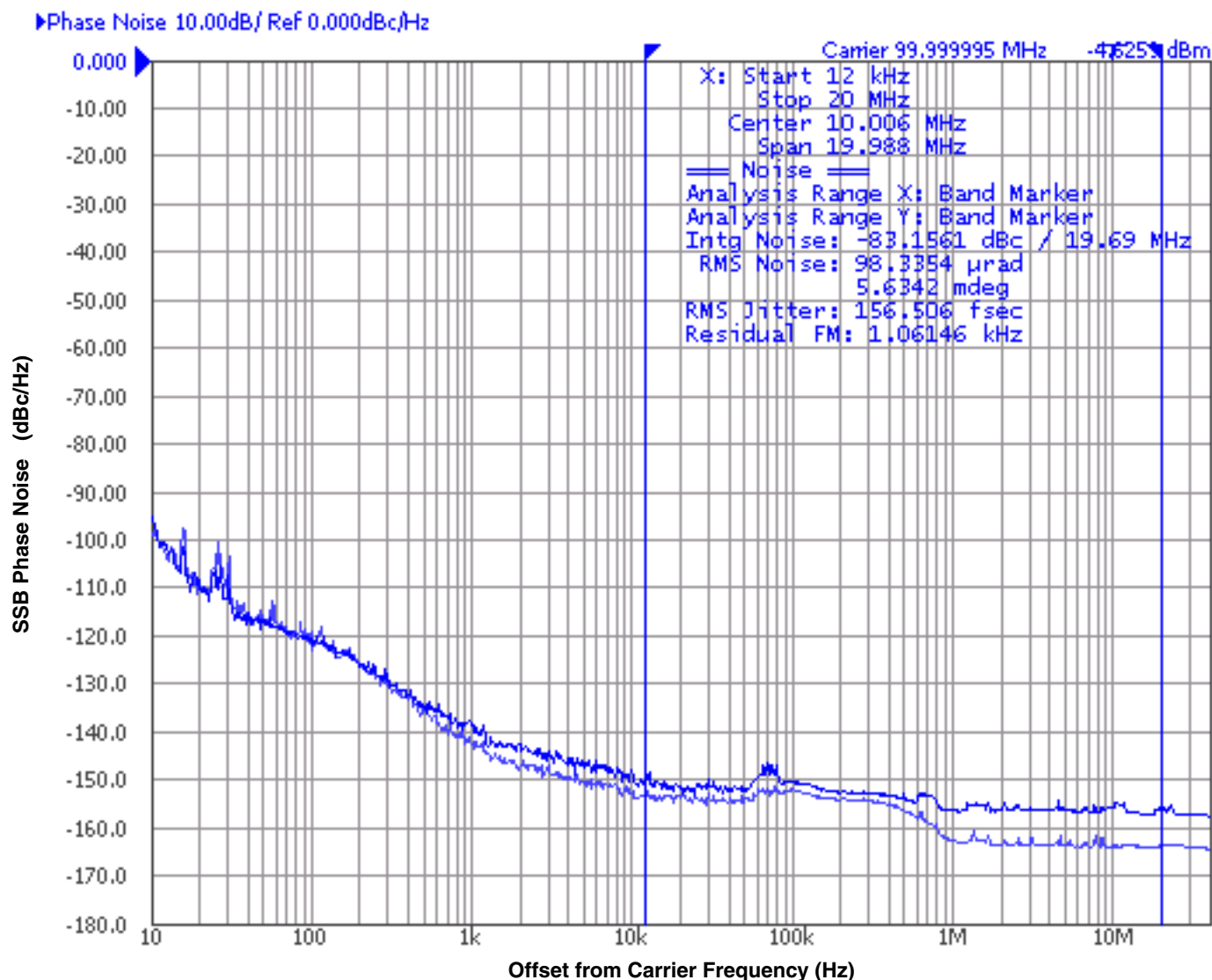
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Each device uses the same type of input.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

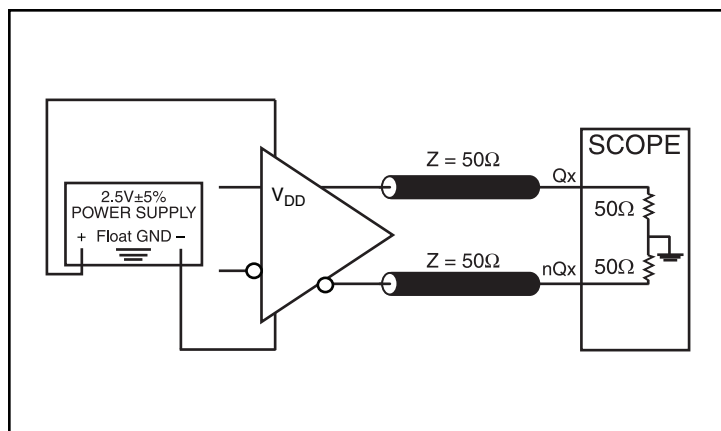


As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

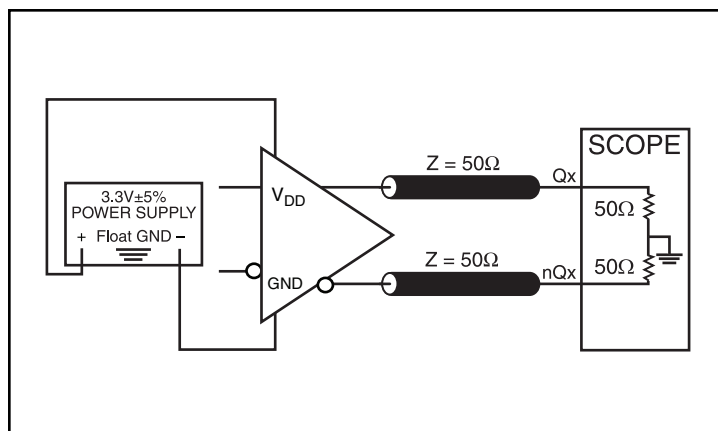
Measured using an Rohde & Schwarz SMA100 as the input source.



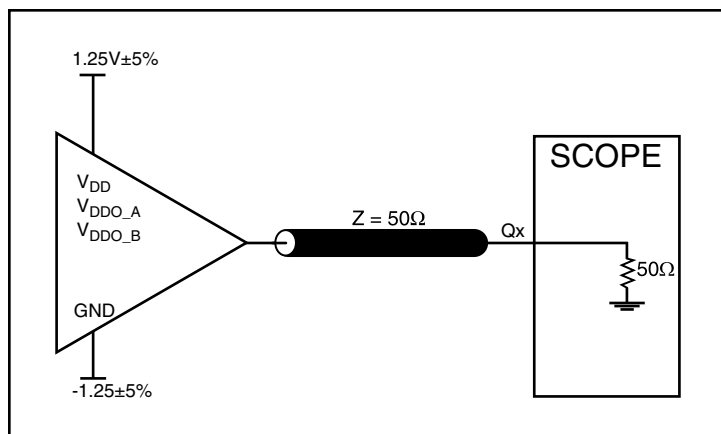
## Parameter Measurement Information



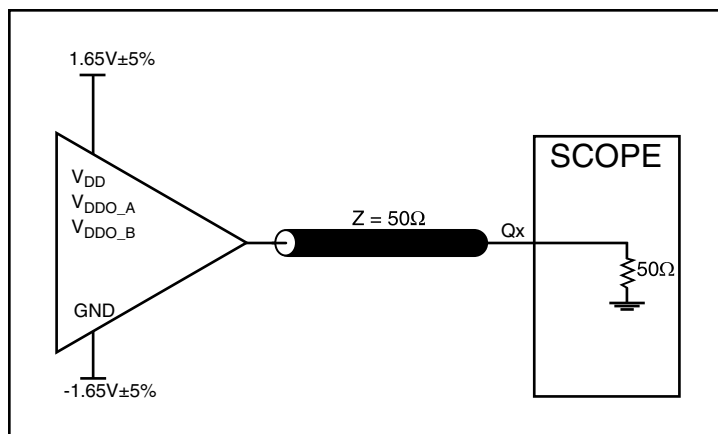
2.5V LVDS Output Load Test Circuit



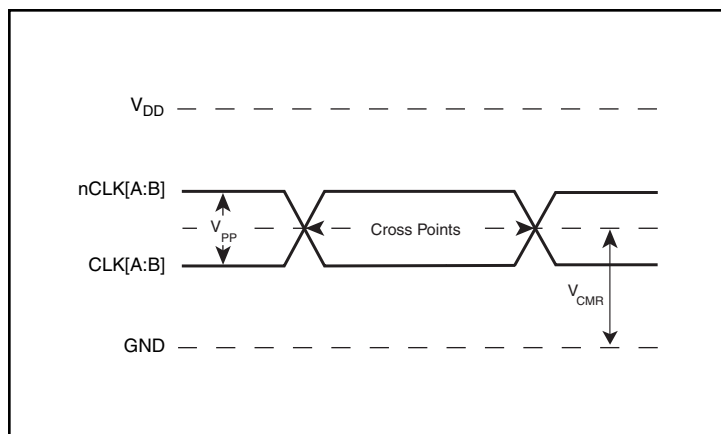
3.3V LVDS Output Load Test Circuit



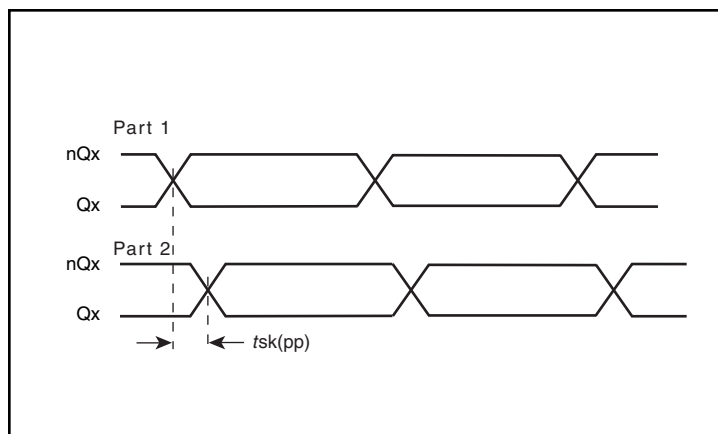
2.5V Core/2.5V LVCMOS Output Load Test Circuit



3.3V Core/3.3V LVCMOS Output Load Test Circuit

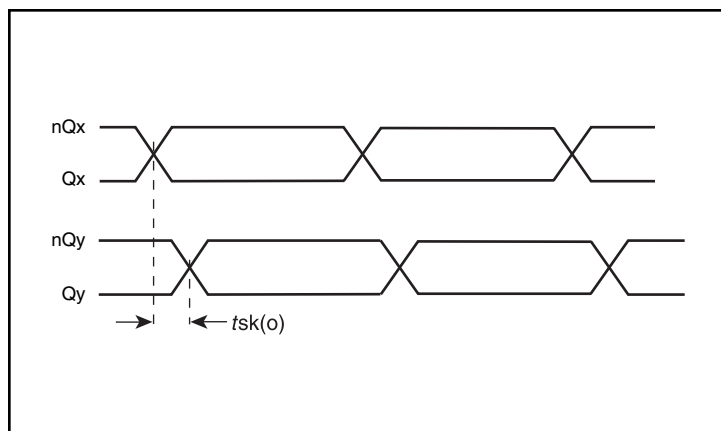


Differential Input Level

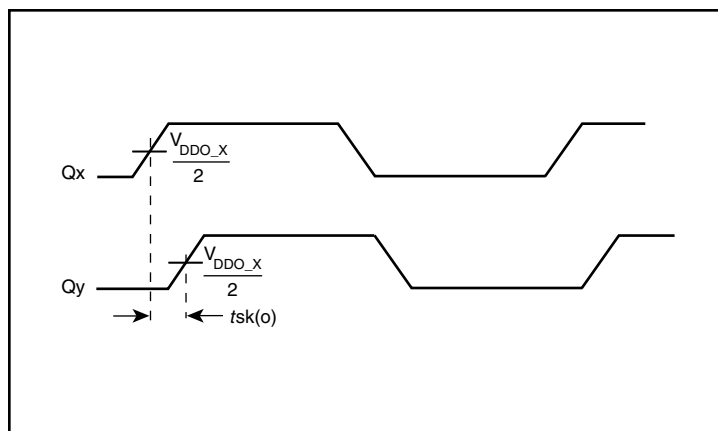


Part-to-Part Skew

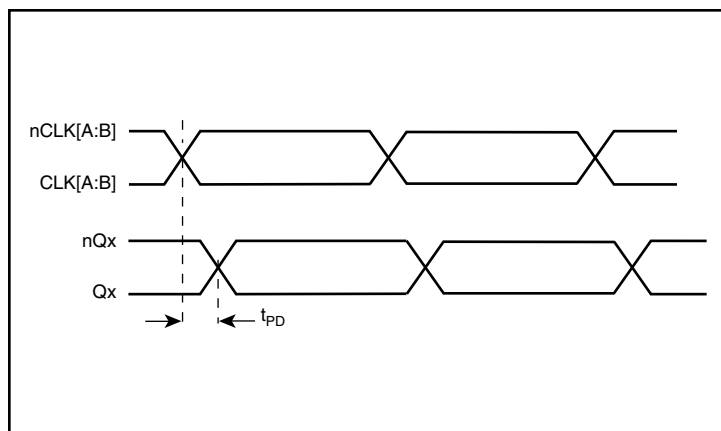
## Parameter Measurement Information, Continued



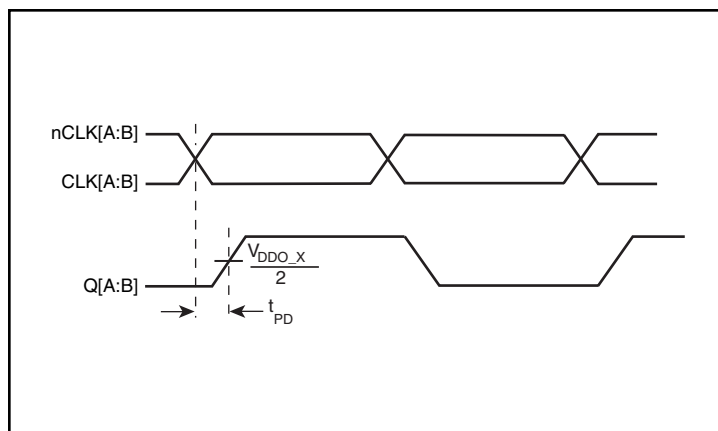
LVDS Output Skew



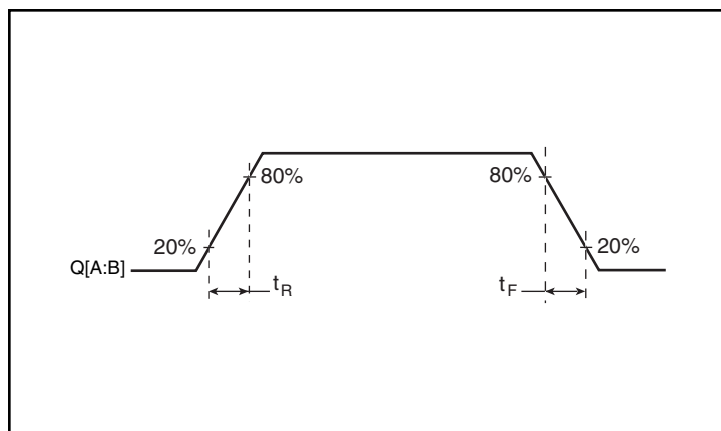
LVCMOS Output Skew



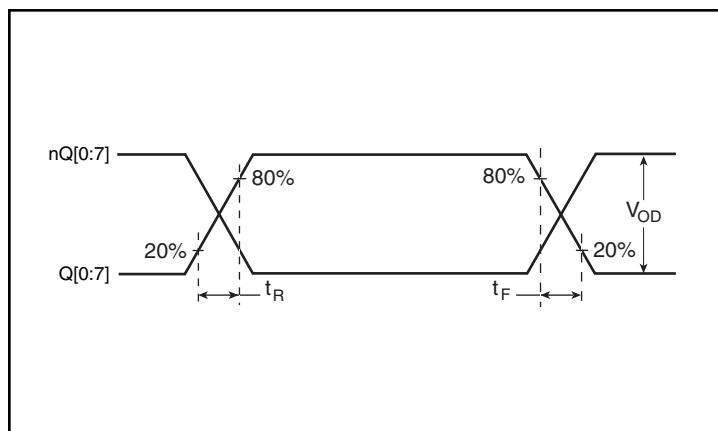
Differential Propagation Delay



Propagation Delay

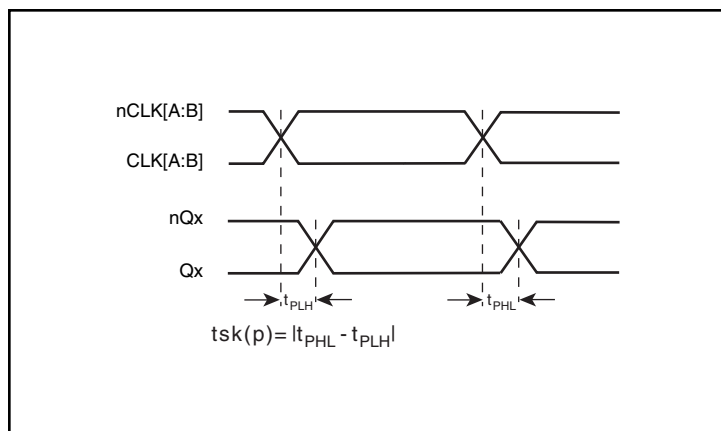


LVCMOS Output Rise/Fall Time

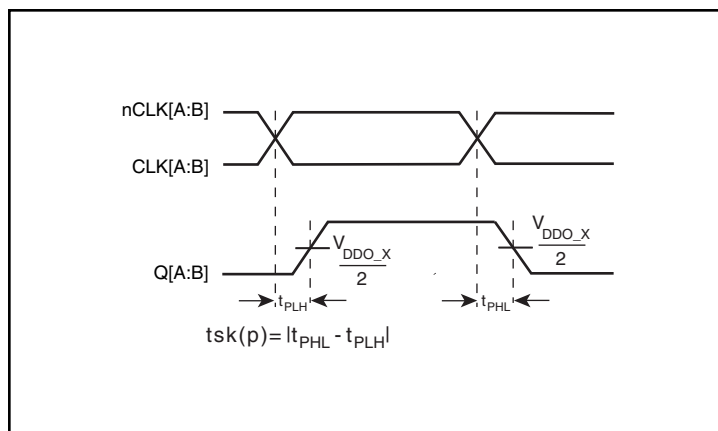


LVDS Output Rise/Fall Time

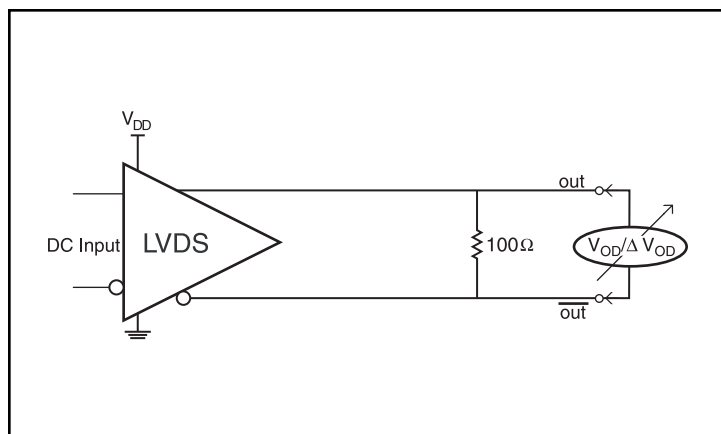
## Parameter Measurement Information, Continued



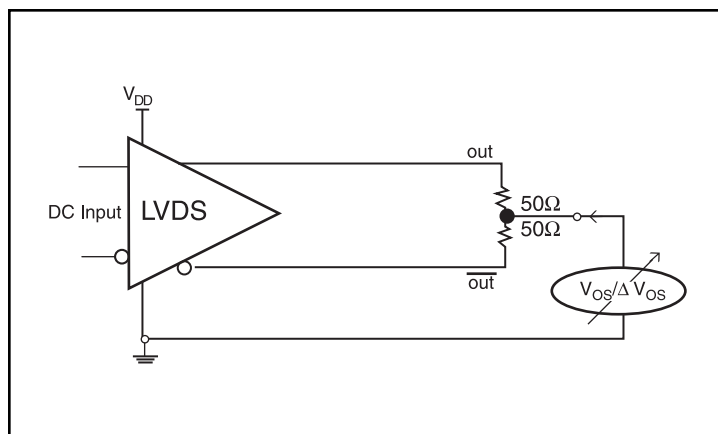
Differential Pulse Skew



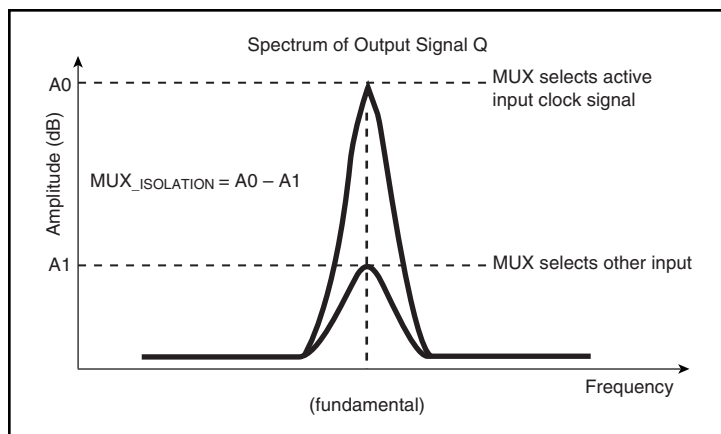
Pulse Skew



Differential Output Voltage Setup



Offset Voltage Setup



MUX Isolation

## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{DD}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{DD} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line

impedance. For most  $50\Omega$  applications, R3 and R4 can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3V$  and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

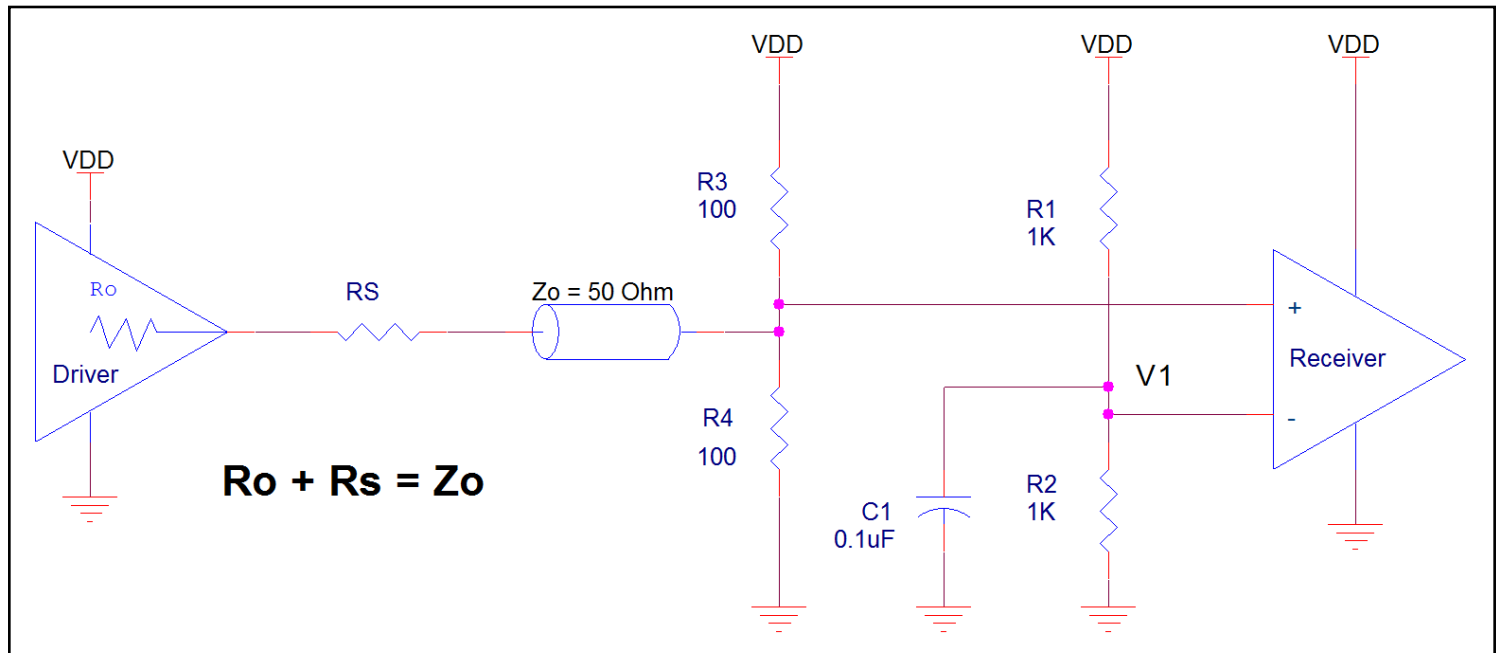
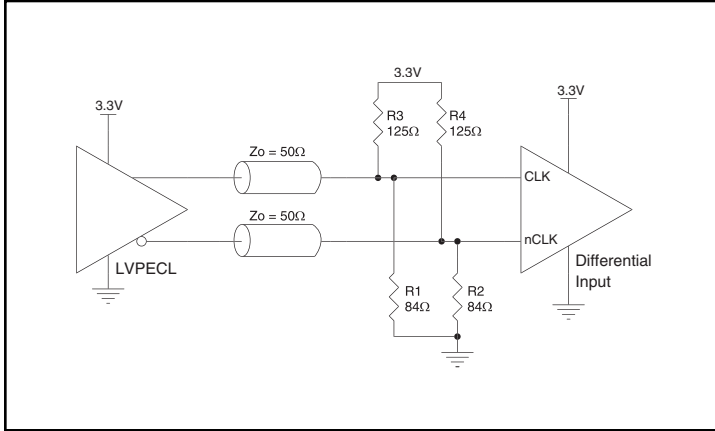


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

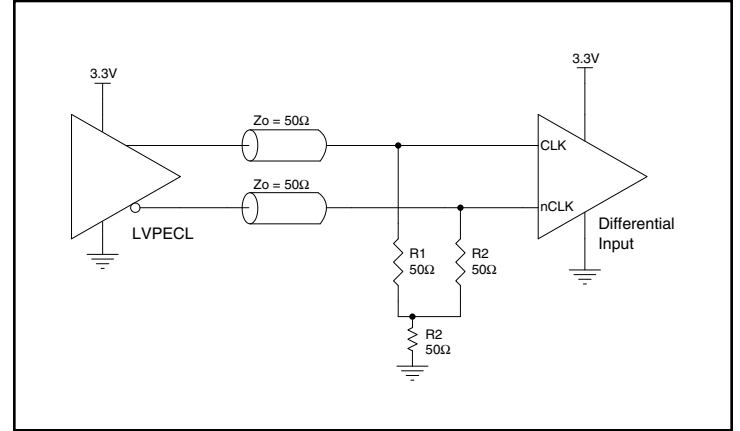
### 3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. [Figure 2A](#) to [Figure 2C](#) show interface examples for the CLK/nCLK input with built-in 50 $\Omega$  terminations driven by the most

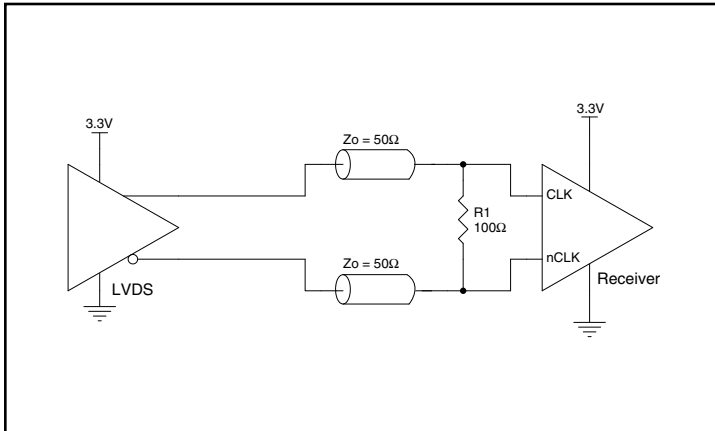
common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

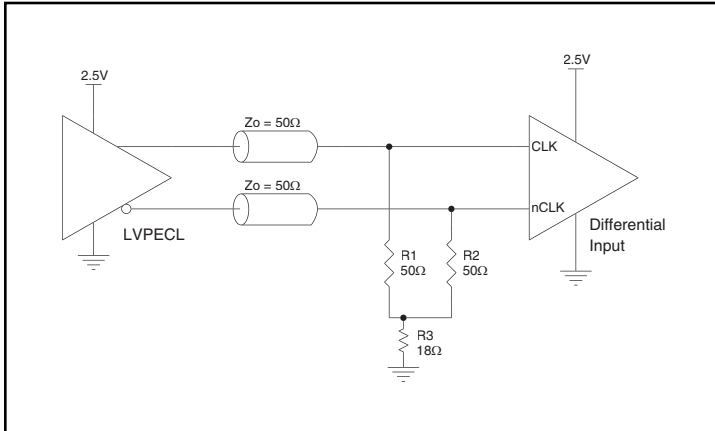


**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

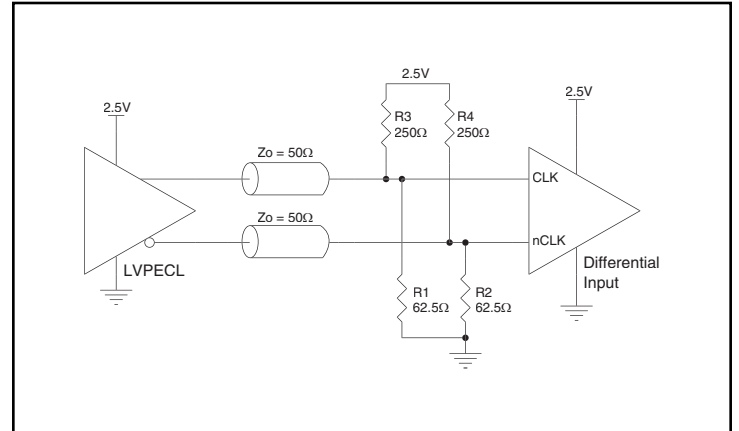
## 2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. [Figure 3A](#) to [Figure 3C](#) show interface examples for the CLK/nCLK input with built-in 50 $\Omega$  terminations driven by the most

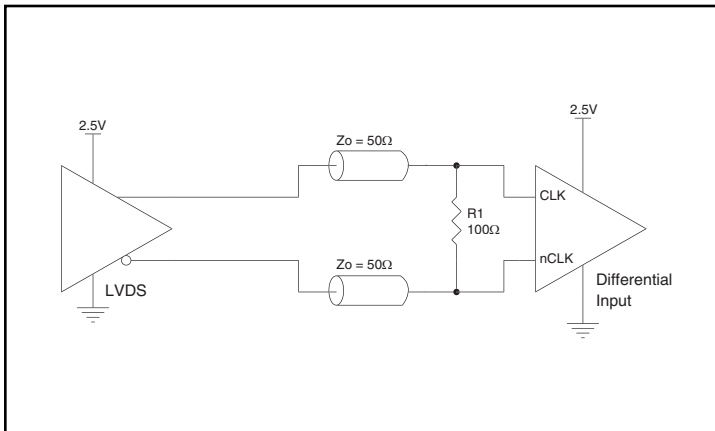
common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 3A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**



**Figure 3C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver**



**Figure 3B. CLK/nCLK Input Driven by a 2.5V LVDS Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVC MOS Control Pins

All control pins have internal pulldown resistors; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### CLK/nCLK Input

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground.

### Outputs:

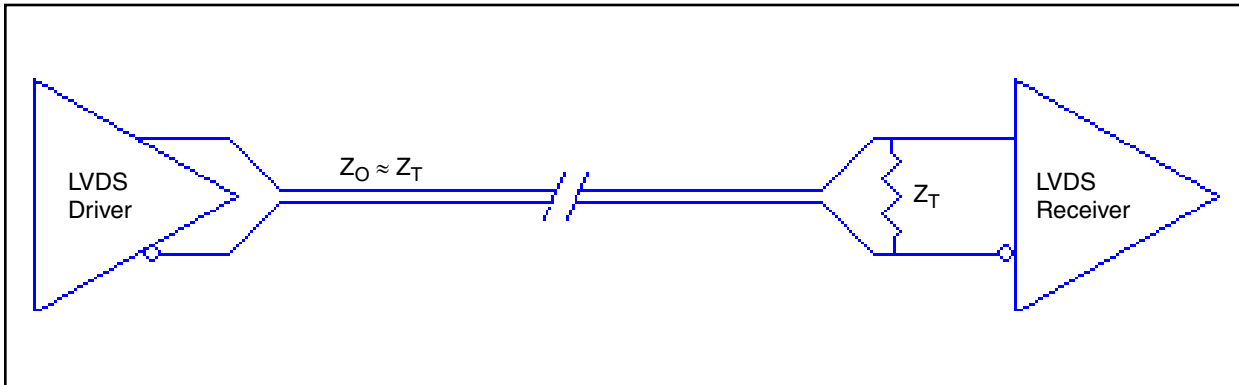
#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating there should be no trace attached.

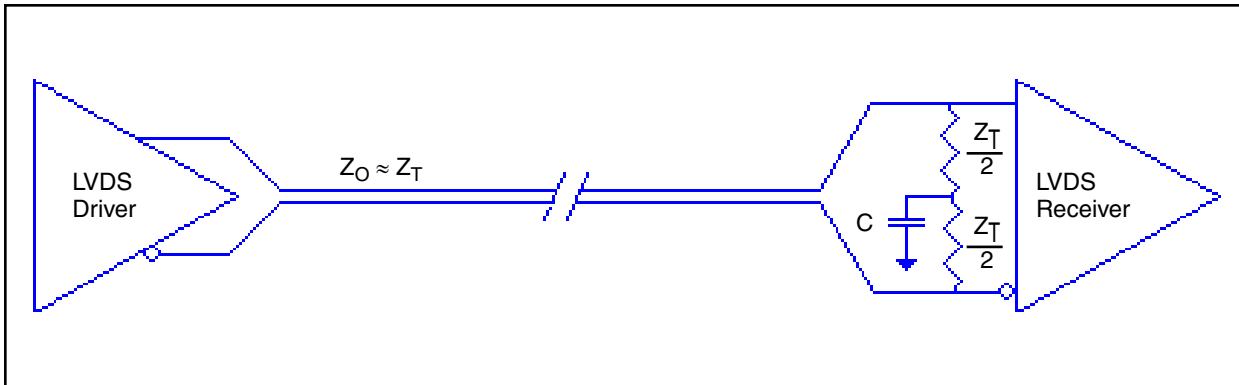
## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output. The standard termination schematic as shown in [Figure 4A](#) can be used

with either type of output structure. [Figure 4B](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



**Figure 4A. Standard Termination**



**Figure 4B. Optional Termination**



## Power Considerations – LVDS Outputs

This section provides information on power dissipation and junction temperature for the 8V34S208. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8V34S208 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

The maximum current at 85°C is as follows:

$$I_{DD} = 184mA$$

$$I_{DDOA} = 4mA$$

$$I_{DDOB} = 4mA$$

- Power (core, LVDS)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDOA\_MAX} + I_{DDOB\_MAX})$   
 $= 3.465V * (184mA + 4mA + 4mA) = \mathbf{665.28mW}$

### LVCMOS Output Power Dissipation

- Dynamic Power Dissipation at 200MHz

$$\text{Power (250MHz)} = CPD * \text{Frequency} * (V_{DDOX\_MAX})^2 = 6pF * 250MHz * (3.465V)^2 = \mathbf{18.01mW \text{ per output}}$$

$$\text{Total CMOS Power} = 2 * 18.01mW = \mathbf{36.02mW}$$

$$\text{Total Power}_{MAX} = 665.28mW + 36.02mW = \mathbf{701.3mW}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

$$\text{The equation for } T_j \text{ is as follows: } T_j = \theta_{JA} * Pd\_total + T_A$$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 48.9°C/W per [Table 7](#) below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.701W * 48.9^\circ C/W = 119.29^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 32-Lead VFQFN**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	48.9°C/W	42.0°C/W	39.4°C/W

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32-Lead VFQFN**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	48.9°C/W	42.0°C/W	39.4°C/W

## Transistor Count

The transistor count for the 8V34S208 is: 492



## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V34S208NLGI	IDT8V34S208NLGI	"Lead-Free" 32-Lead VFQFN	Tray	-40°C to 85°C
8V34S208NLGI8	IDT8V34S208NLGI	"Lead-Free" 32-Lead VFQFN	Tape & Reel	-40°C to 85°C



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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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