

## General Description

The 845264 is a 3.3V, 2.5V CML clock generator designed for Ethernet applications. The device synthesizes four clock frequencies on two separately selectable output banks. Each bank has either a 62.5MHz, 125MHz, 156.25MHz or 312.5MHz clock signal with excellent phase jitter performance. Each clock frequency is distributed to two low-skew differential CML output banks with a total of four outputs. The device is suitable for driving the reference clocks of Ethernet PHYs. The device supports 3.3V and 2.5V voltage supply and is packaged in a small, lead-free (RoHS 6) 32-lead VFQFN package. The extended temperature range supports telecommunication, wireless infrastructure and networking end equipment requirements.

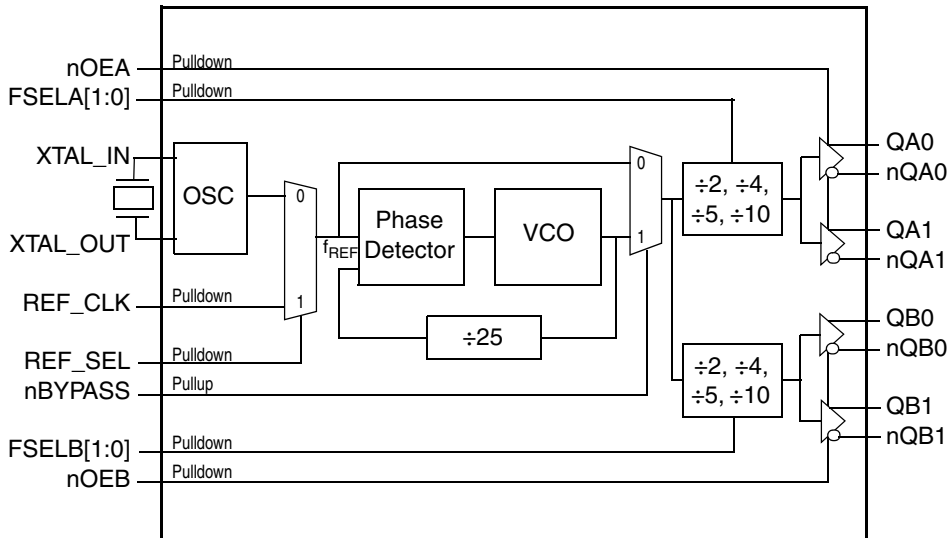
## Features

- Clock generation of: 62.5MHz, 125MHz, 156.25MHz and 312.5MHz
- Two banks of two differential CML clock outputs
- Crystal interface designed for 25MHz, 12pF parallel resonant crystal
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.486ps (typical)

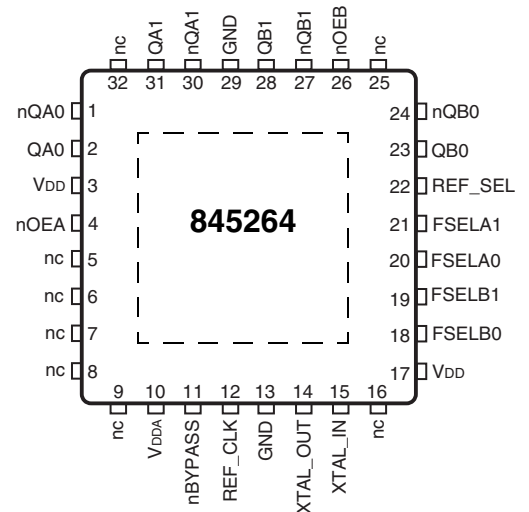
Offset	Single-side Band Phase Noise
100Hz .....	-97 dBc/Hz
1kHz.....	-118 dBc/Hz
10kHz.....	-125 dBc/Hz
100kHz.....	-123 dBc/Hz

- LVCMOS interface levels for the control inputs
- Full 3.3V and 2.5V supply voltage
- Lead-free (RoHS 6) 32 VFQFN packaging
- -40°C to 85°C ambient operating temperature

## Block Diagram



## Pin Assignment



32 lead, 5mm x 5mm VFQFN

## Pin Descriptions and Characteristics

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	nQA0, QA0	Output		Bank A differential clock output pair. CML interface levels.
3, 17	V <sub>DD</sub>	Power		Core supply pins.
4	nOEA	Input	Pulldown	Output enable pin for Bank A outputs. See Table 3E for function. LVCMOS/LVTTL interface levels.
5, 6, 7, 8, 9, 16, 25, 32	nc	Unused		Do not connect.
10	V <sub>DDA</sub>	Power		Analog supply pin.
11	nBYPASS	Input	Pullup	PLL bypass pin. See Table 3D for function. LVCMOS/LVTTL interface levels.
12	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
13, 29	GND	Power		Power supply ground.
14, 15	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
18, 19	FSELB0, FSELB1	Input	Pulldown	Output frequency divider select enable pins for Bank B outputs. See Table 3C for function. LVCMOS/LVTTL interface levels.
20, 21	FSELA0, FSELA1	Input	Pulldown	Output frequency divider select enable pins for Bank A outputs. See Table 3B for function. LVCMOS/LVTTL interface levels.
22	REF_SEL	Input	Pulldown	PLL reference clock select pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
23, 24	QB0, nQB0	Output		Bank B differential clock output pair. CML interface levels.
26	nOEB	Input	Pulldown	Output enable pin for Bank B outputs. See Table 3F for function. LVCMOS/LVTTL interface levels.
27, 28	nQB1, QB1	Output		Bank B differential clock output pair. CML interface levels.
30, 31	nQA1, QA1	Output		Bank A differential clock output pair. CML interface levels.

NOTE: *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance	nBYPASS, REF_SEL, nOEA, nOEB, FSELB0, FSELB1, FSELA0, FSELA1			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor				51		kΩ
R <sub>PULLUP</sub>	Input Pullup Resistor				51		kΩ

## Function Tables

**Table 3A. PLL Reference Clock Select Function Table**

Input	Operation
REF_SEL	
0 (default)	The crystal interface is the selected reference clock.
1	The REF_CLK input is the selected reference clock.

NOTE: REF\_SEL is an asynchronous control.

**Table 3B. FSELA[1:0] Output Divider Select Function Table**

Input		Operation	Output Frequency
FSELA1	FSELA0		
0 (default)	0 (default)	$\div 2$	312.5MHz
0	1	$\div 4$	156.25MHz
1	0	$\div 5$	125MHz
1	1	$\div 10$	62.5MHz

NOTE: FSELA[1:0] are asynchronous controls. Using 25MHz input reference.

**Table 3C. FSELB[1:0] Output Divider Select Function Table**

Input		Operation	Output Frequency
FSELB1	FSELB0		
0 (default)	0 (default)	$\div 2$	312.5MHz
0	1	$\div 4$	156.25MHz
1	0	$\div 5$	125MHz
1	1	$\div 10$	62.5MHz

NOTE: FSELB[1:0] are asynchronous controls. Using 25MHz input reference.

**Table 3D. PLL nBYPASS Function Table**

Input	Operation
nBYPASS	
0	PLL is bypassed. The reference frequency $f_{REF}$ is divided by the selected output divider. AC specifications do not apply in PLL bypass mode.
1 (default)	PLL is enabled. The reference frequency $f_{REF}$ is multiplied by the selected feedback divider and then divided by the selected output divider.

NOTE: nBYPASS is an asynchronous control.

**Table 3E. Output Enable Function Table**

Input	Operation
nOEA	
0 (default)	QA[1:0], nQA[1:0] Outputs enabled.
1	QA[1:0], nQA[1:0] Outputs disabled (high-impedance).

NOTE: nOEA is an asynchronous control.

**Table 3F. Output Enable Function Table**

Input	Operation
nOEB	
0 (default)	QB[1:0], nQB[1:0] Outputs enabled.
1	QB[1:0], nQB[1:0] Outputs disabled (high-impedance).

NOTE: nOEB is an asynchronous control.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to $V_{DD}$ -0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	43.4°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.12$	3.3	$V_{DD}$	V
$I_{DD}$	Power Supply Current			71	89	mA
$I_{DDA}$	Analog Supply Current			9	12	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.11$	2.5	$V_{DD}$	V
$I_{DD}$	Power Supply Current			68	84	mA
$I_{DDA}$	Analog Supply Current			8	11	mA

**Table 4C. LVCMOS/LVTTL Input DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$V_{DD} = 3.3V$	2.2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		$V_{DD} = 3.3V$	-0.3		0.8	V
			$V_{DD} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	nOEA, nOEB, FSELA[1:0], FSELB[1:0], REF_SEL, REF_CLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
		nBYPASS	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	nOEA, nOEB, FSELA[1:0], FSELB[1:0], REF_SEL, REF_CLK	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$
		nBYPASS	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$

**Table 4D. CML DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{DD} - 0.02$	$V_{DD} - 0.01$	$V_{DD}$	V
$V_{OUT}$	Output Voltage Swing		300	480	600	mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing		600	960	1200	mV

NOTE 1: Outputs are terminated with  $50\Omega$  to  $V_{DD}$ .

**Table 5. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance ( $C_O$ )				7	pF
Load Capacitance ( $C_L$ )				12	pF

## AC Characteristics

**Table 6. AC Characteristics**,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency; NOTE 1	FSELx[1:0] = 00		312.5		MHz
		FSELx[1:0] = 01		156.25		MHz
		FSELx[1:0] = 10		125		MHz
		FSELx[1:0] = 11		62.5		MHz
tsk(o)	Output Skew; NOTE 1, 2, 3				80	ps
tsk(b)	Bank Skew; NOTE 1, 3, 4				30	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter; NOTE 5, 6	125MHz, Integration Range: 1.875MHz – 20MHz		0.486		ps
		156.25MHz, Integration Range: 1.875MHz – 20MHz		0.427		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300	480	800	ps
odc	Output Duty Cycle		45	50	55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1:  $f_{REF} = 25\text{MHz}$ . Outputs are terminated with  $50\Omega$  to  $V_{DD}$ . (FOX 277LF-25-99, 12pF, 25MHz crystal)

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoint.

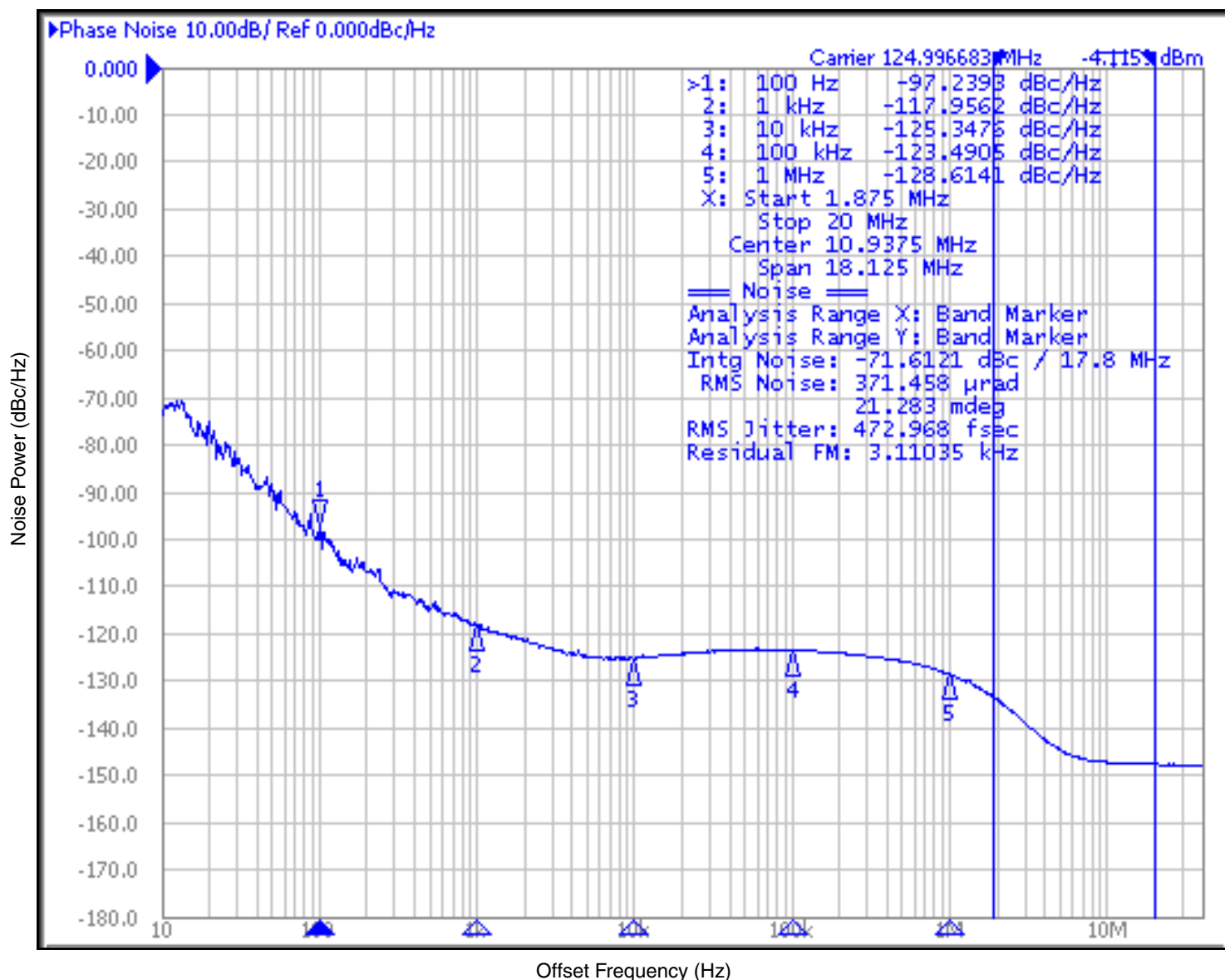
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

NOTE 5: Please refer to the phase noise plots.

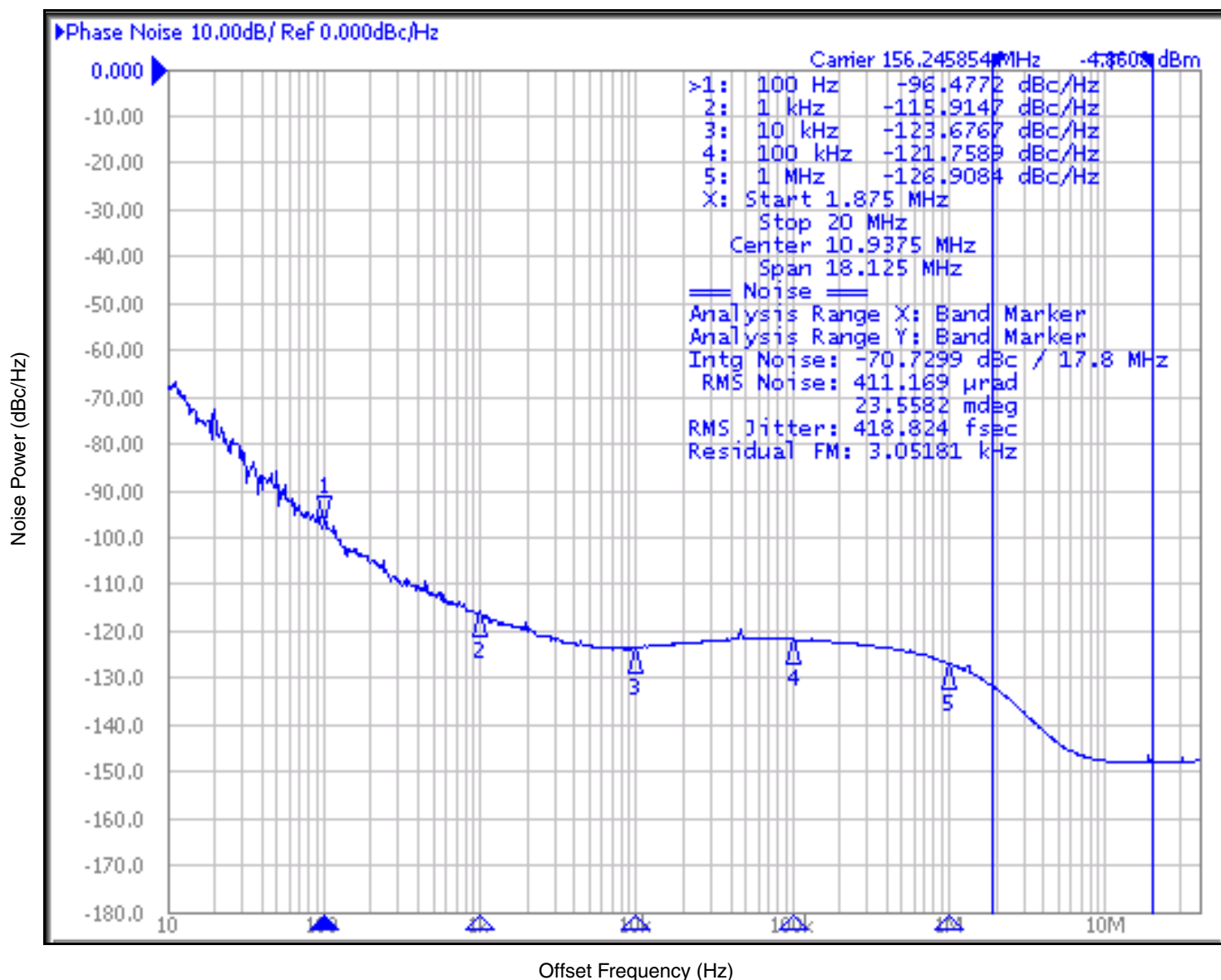
NOTE 6: Data was taken with both outputs at the same frequency.

# Typical Phase Noise at 125MHz

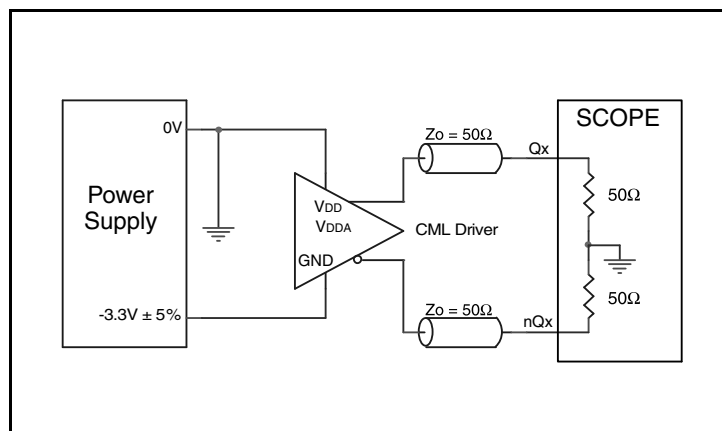




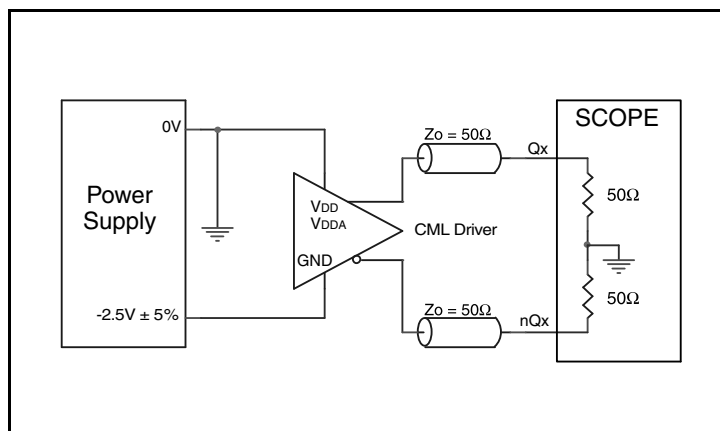
# Typical Phase Noise at 156.25MHz



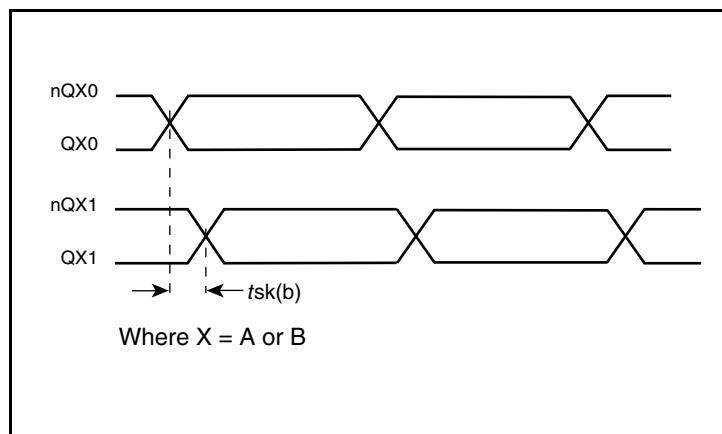
## Parameter Measurement Information



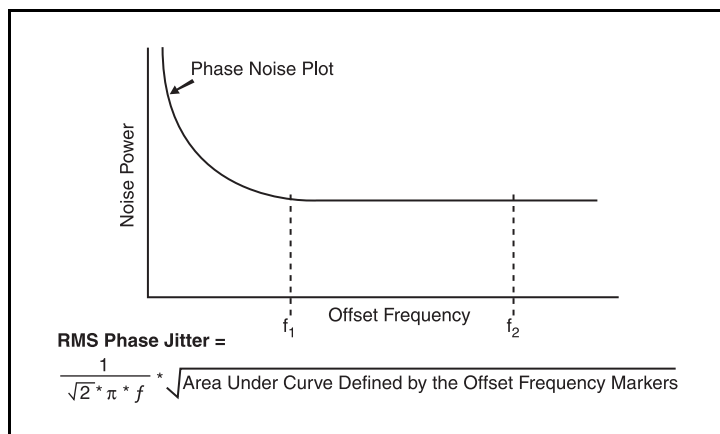
3.3V CML Output Load Test Circuit



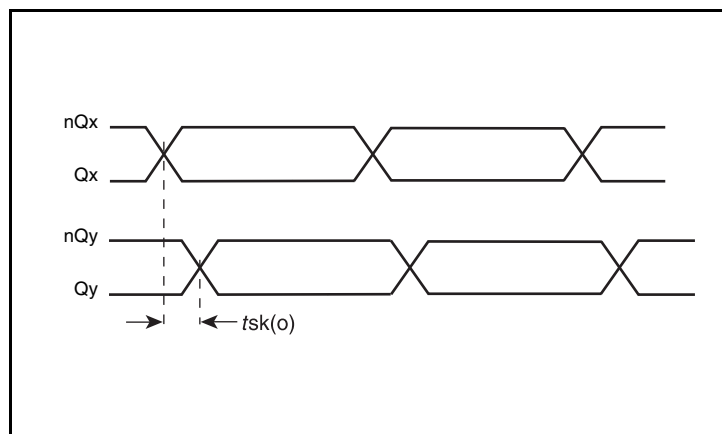
2.5V CML Output Load Test Circuit



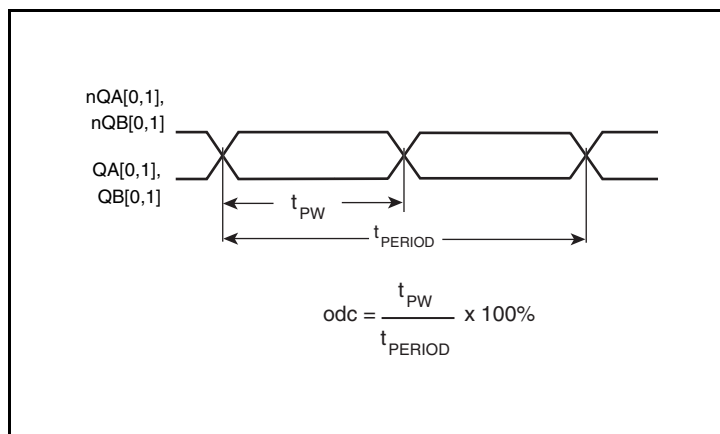
Bank Skew



RMS Phase Jitter

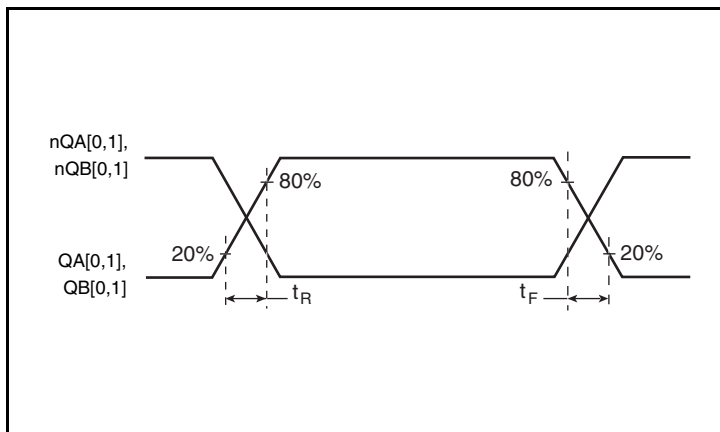


Output Skew

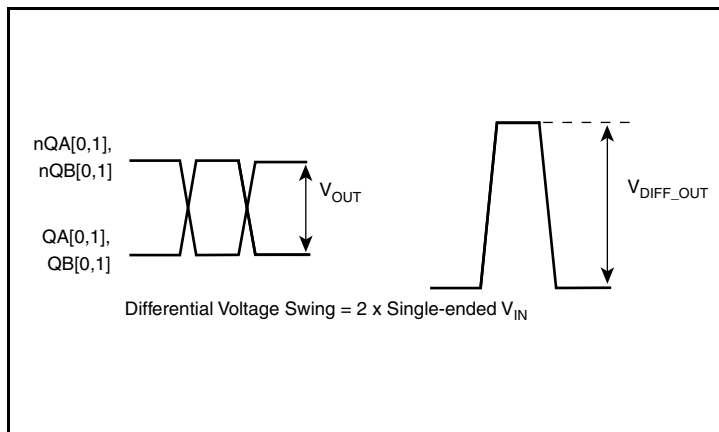


Output Duty Cycle/Pulse Width/Period

## Parameter Measurement Information, continued



Output Rise/Fall Time



Differential Output Voltage Swing

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

##### REF\_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the REF\_CLK to ground.

#### Outputs:

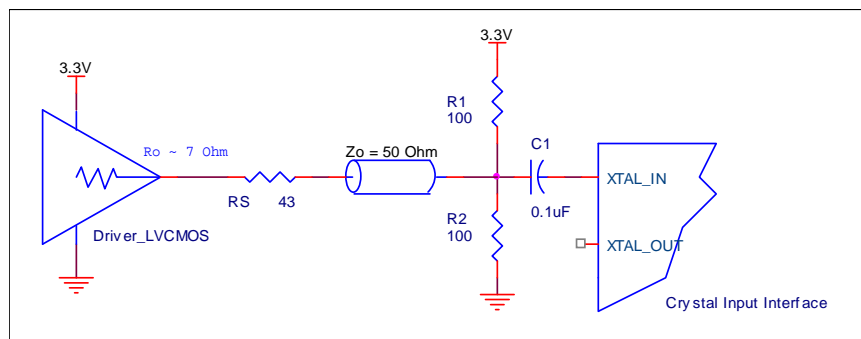
##### CML Outputs

All unused CML outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

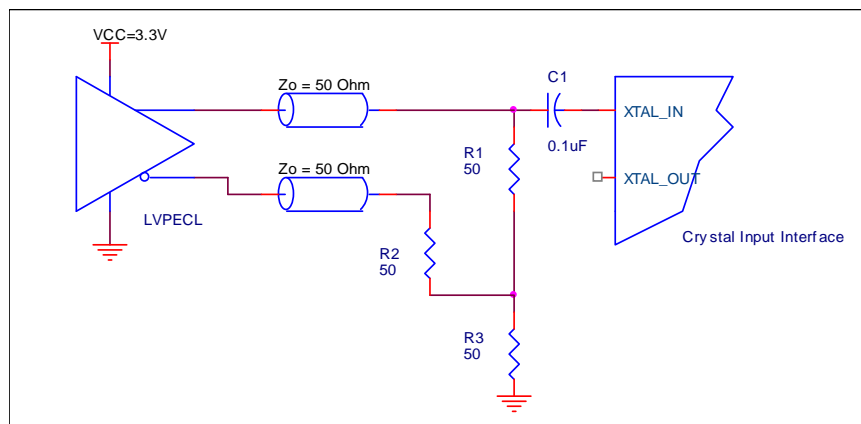
## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVC MOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVC MOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVC MOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50 $\Omega$  applications,  $R_1$  and  $R_2$  can be 100 $\Omega$ . This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50 $\Omega$ . The values of the resistors can be increased to reduce the loading for a slower and weaker LVC MOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.



**Figure 1A. General Diagram for LVC MOS Driver to XTAL Input Interface**



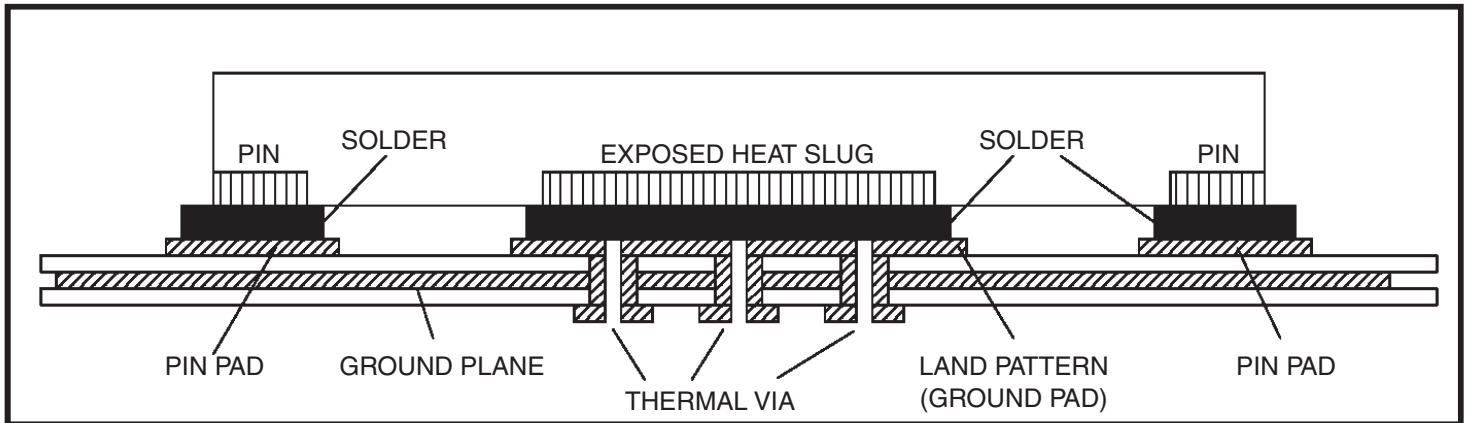
**Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 2. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Schematic Example

Figure 3 shows an example of 845264 application schematic. In this example, the device is operated at  $V_{DD} = V_{DDA} = 3.3V$ . The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

A 12pF parallel resonant 25MHz crystal is used. For this device, the crystal load capacitors are required for proper operation. The load capacitance,  $C1 = C2 = 2pF$ , are recommended for frequency accuracy. Depending on the variation of the parasitic stray capacity of the printed circuit board traces between the crystal and the XTAL\_IN and XTAL\_OUT pins, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2. When designing the circuit board, return the capacitors to ground through a single point contact close to the package. Two Fox crystal options are shown in the schematic for design flexibility.

The ePAD provides a low thermal impedance connection between the internal device and the PCB. It also provides an electrical connection to the die and must be connected to ground.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 845264 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

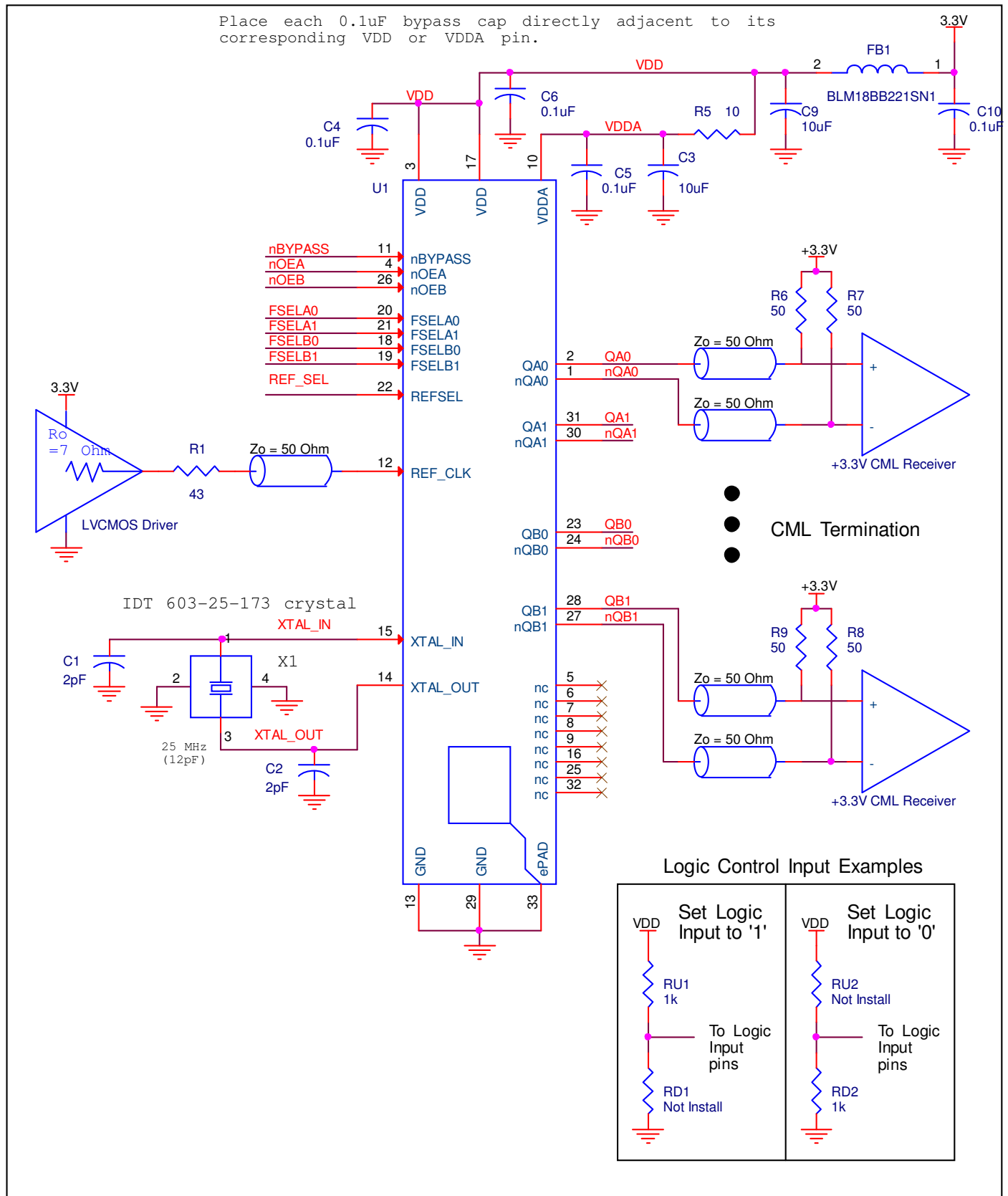


Figure 3. 845264 Schematic Example



## Power Considerations

This section provides information on power dissipation and junction temperature for the 845264. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 845264 is the sum of the core power plus the power dissipation into the load. The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation into the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (89mA + 12mA) = \mathbf{349.96mW}$
- Power (outputs)<sub>MAX</sub> = **35.76mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 35.76mW = \mathbf{143.04mW}$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $349.96mW + 143.04mW = \mathbf{493.00mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 43.4°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.493W * 43.4^\circ\text{C/W} = 106.4^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

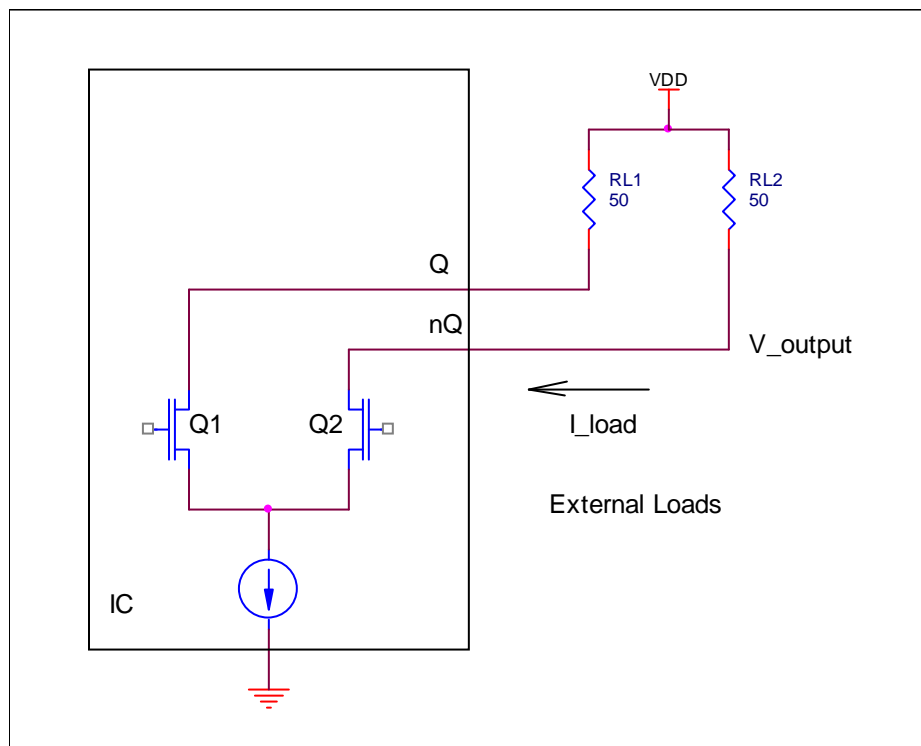
This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the CML driver output pair. The CML output circuit and termination are shown in Figure 4.



**Figure 4. CML Driver Circuit and Termination**

To calculate power dissipation per output pair into the load, use the following equations.

Power dissipation when the output driver is logic LOW:

$$\begin{aligned}
 Pd\_L &= I_{Load} * V\_Output \\
 &= (V_{OUT\_MAX} / R_L) * (V_{DD\_MAX} - V_{OUT\_MAX}) \\
 &= (600mV / 50\Omega) * (3.465V - 600mV) \\
 &= 34.38mW
 \end{aligned}$$

Power dissipation when the output driver is logic HIGH:

$$\begin{aligned}
 Pd\_H &= I_{Load} * V\_Output \\
 &= (0.02V / 50\Omega) * (3.465V - 0.02V) \\
 &= 1.38mW
 \end{aligned}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{35.76mW}$$

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32 lead VFQFN**

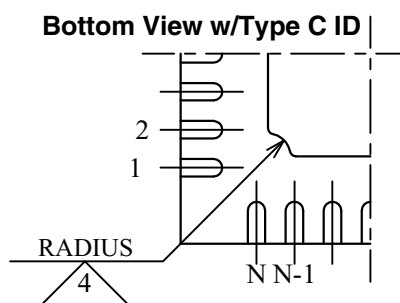
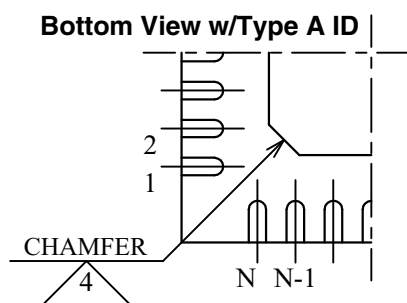
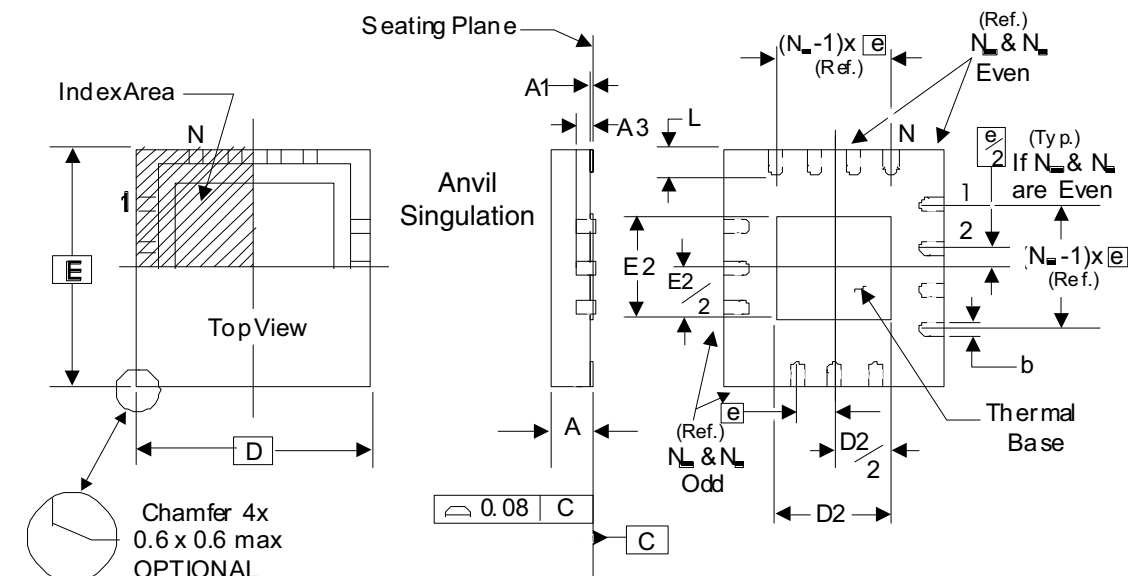
$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

## Transistor Count

The transistor count for the 845264 is: 3216

# 32 Lead VFQFN Package Outline and Package Dimensions

## Package Outline - K Suffix for 32 Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

**Table 9. Package Dimensions**

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A	0.80		1.00
A1	0		0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
$N_D$ & $N_E$	8		
D & E	5.00 Basic		
D2 & E2	3.0		3.3
e	0.50 Basic		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 9.

## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
845264AKILF	ICS45264AIL	32 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
845264AKILFT	ICS45264AIL	32 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		16	Updated schematic with IDT crystal recommendation. Deleted prefix/suffix from part number throughout the datasheet. Updated header/footer.	7/20/15



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.