RL78/G13

Safety Function (A/D Test) CC-RL

Introduction

This application note explains the sample code for the A/D test function, which is one of the safety functions of the RL78/G13.

The A/D test function performs A/D conversions at three reference voltage points to check the A/D converter for normal operation. The three reference voltage points are the internal 0 V, VDD, and internal reference voltage (1.45 V).

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

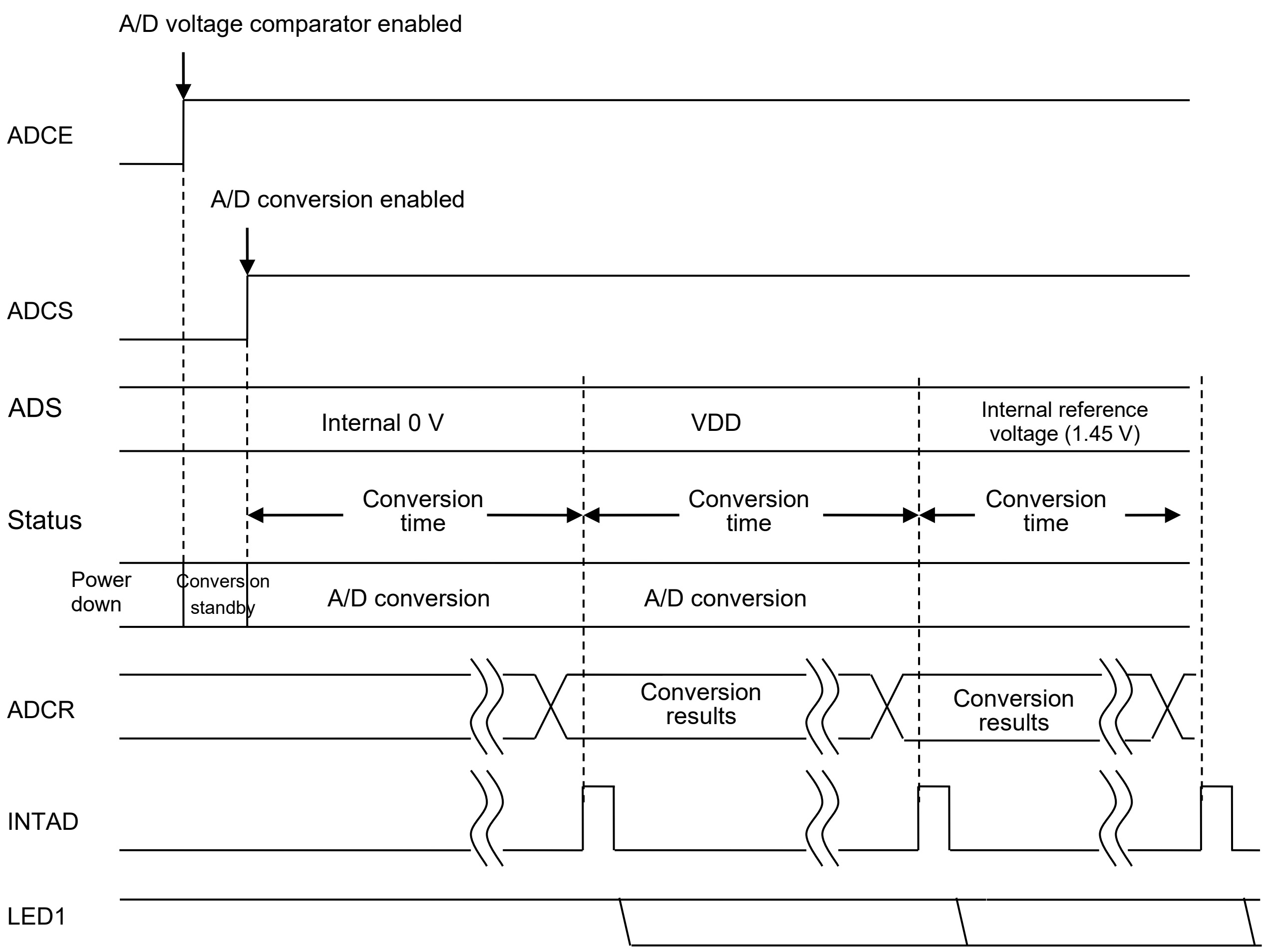
1. Specifications

This application note contains an example of using the A/D test function, which is one of the safety functions of the RL78/G13. The sample code covered in this application note converts internal 0 V, VDD, and internal reference voltage (1.45 V) to digital values. Subsequently, it turns on LED1 if the conversion results are within the allowable range and blinks it otherwise.

Table 1.1 summarizes peripheral functions to be used. Figure 1.1 shows the outline of the conversion of the A/D converter.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
A/D converter	Converts analog signal inputs at the levels that are referred to as internal 0 V, VDD, and internal reference voltage (1.45 V) to digital values.
Bit 2 of port 6	Used to output the A/D conversion results to LED1.



LED1 is turned on if the A/D conversion results are within the allowable range and blinked otherwise.

If the conversion results are outside the allowable range, the sample code halts the A/D test immediately, without changing the test voltage to the next test voltage level, and keeps LED1 blinking.

Figure 1.1 Outline of Conversion of the A/D Converter

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V LVD operation (V_{LVD}): Reset mode 4.06 V +/- 0.08 V
Integrated development environment (CS+)	CS+ for CC V8.05.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.10.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V2021-04 (21.4.0) from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.10.00 from Renesas Electronics Corp.

3. Related Application Notes

The application note that are related to this application note are listed below for reference.

RL78/G13 Initialization (R01AN2575E) Application Note
RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) (R01AN2581E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

The example of configuration of the hardware that is used for this application note is shown below.

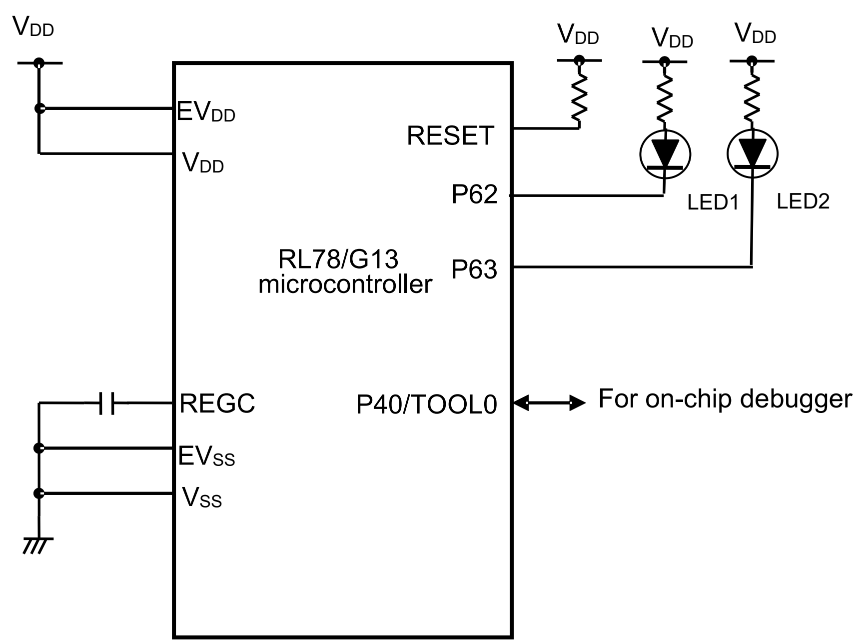


Figure 4.1 Hardware Configuration

Notes: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4. LED2 connected to P63 is always off.

4.2 List of Pins to be used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P62	Output	Outputs the A/D conversion results to LED1.

5. Description of the Software

5.1 Operation Outline

This sample code performs A/D conversions on the analog voltages at the internal 0 V, VDD, and internal reference voltage (1.45 V) sequentially using the software trigger and sequential conversion modes of the A/D converter. It then waits for the completion of the A/D conversion in HALT mode. After the A/D conversion is finished, the sample code checks to determine if the A/D conversion results are within the allowable range. It turns on LED1 if the conversion results are within the allowable range and blinks it otherwise.

(1) Initialize the A/D converter.
<Setup conditions>

- Supply the input clock to the A/D converter.
- Set A/D conversion channel selection mode to select mode.
- Set A/D conversion operation mode to sequential conversion mode.
- Start A/D conversion by using the software trigger.
- Use the A/D conversion end interrupt (INTAD).

(2) Switch the test voltage.
Switch the register settings according to the test voltage to be used for A/D conversion.

More specifically, perform the following steps:

- Disable the A/D voltage comparator.

<When the test voltage is internal 0 V>

- Set the A/D test target to the internal 0 V.

< When the test voltage is VDD>

- Set the A/D test target to VDD.

< When the test voltage is internal reference voltage >

- Set the A/D test target to the internal reference voltage.
- Enable the A/D voltage comparator and wait for a stabilization period (1 us).

(3) Start A/D conversion.
Set the ADCS bit in the ADM0 register to 1 (Starts conversion operation) to start A/D conversion.

(4) Execute the HALT instruction to enter the HALT mode and wait for an A/D conversion end interrupt.
When the A/D conversion on the input voltage is finished, the A/D converter transfers the A/D conversion results to the ADCR register and generates an A/D conversion end interrupt.

(5) Check the A/D conversion results.
When the sample code exits the HALT mode on the A/D conversion end interrupt, it reads the A/D conversion results from the ADCR register.

(6) Check to determine if the A/D conversion results are within the allowable range.
<If the A/D conversion results are within the allowable range >

- If the tests on the three types of input voltages are completed, the sample code turns on LED1 and enters an infinite loop.
- If the tests on the three types of input voltages are not completed, the sample code repeats steps (2) to (6).

<If the A/D conversion results are outside the allowable range >

- The sample code enters an infinite loop for blinking LED1.

5.2 File Configuration

Table 5.1 lists the files that are used by the sample code, excluding files that are automatically generated by the integrated development environment.

Table 5.1 File Configuration

File Name	Description	Remarks
r_main.c	Main processing block	Functions added: R_Main_Check_AD_Data, R_Main_Blink_Led
r_adc_user.c	A/D converter module	Functions added: R_ADC_Set_TestVoltage, R_ADC_Set_Vss, R_ADC_Set_Vdd, R_ADC_Set_Vbgr,

5.3 List of Option Byte Settings

Table 5.2 summarizes the settings of the option bytes.

Table 5.2 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01110011B	LVD reset mode, 4.06 V +/- 0.08 V
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

Caution: Do not set the option byte at address C2H to any mode other than HS mode. Normal operation of the function is not guaranteed if a mode other than HS is specified.

5.4 List of Constants

Table 5.3 lists the constants that are used in this sample program.

The initial values are listed in Table 5.3.

Table 5.3 Constants for the Sample Program

Constant	Setting	Description
OVERALL_ERROR_LSB_UNIT	7	Overall A/D converter error ±7 LSB This constant determines the allowable error of the tests.
VSS_RANGE_MAX	7	Upper limit of allowable internal 0 V range Determined by VSS_RANGE_MAX = 0 + OVERALL_ERROR_LSB_UNIT.
AD_RESOLUTION_HEX	0x03FF	A/D conversion resolution = 10 bits
VDD_RANGE_MIN	0x03F8	Lower limit of allowable VDD range Determined by VDD_RANGE_MIN = AD_RESOLUTION_HEX - OVERALL_ERROR_LSB_UNIT.
VDD	5.0	VDD (unit: V)
VBGR_MIN	1.38	Minimum internal reference voltage (1.45 V) (unit: V)
VBGR_MAX	1.5	Maximum internal reference voltage (1.45 V) (unit: V)
VBGR_RANGE_MIN	0x0113	Lower limit of allowable internal reference voltage (1.45 V) Determined by VBGR_RANGE_MIN = (VBGR_MIN / (VDD / 0x03FF)) - OVERALL_ERROR_LSB_UNIT.
VBGR_RANGE_MAX	0x013A	Upper limit of allowable internal reference voltage (1.45 V) Determined by VBGR_RANGE_MAX = (VBGR_MAX / (VDD / 0x03FF)) + OVERALL_ERROR_LSB_UNIT.

Cautions:
1. The constants listed in Table 5.3 are obtained at a power voltage of 5.0 V. Change VDD according to the system.
2. There are cases in which the results of executing the sample code are outside the allowable range when a power voltage of 5.0 V is supplied and the constants listed in Table 5.3 are used (the results of an A/D test performed on the internal reference voltage with the power voltage being supplied from the E1 emulator will go beyond the allowable range). In such a case, replace the power supply with a more stable power supply or determine the allowable range setting while paying attention to the possible errors that may be caused by the power supply (more specifically, adjust OVERALL_ERROR_LSB_UNIT).

Table 5.4 lists the A/D test voltages and the upper and lower limit of their allowable ranges.

The values listed in the table are obtained when the constants listed in Table 5.3 are used.

Table 5.4 A/D Test Voltages and their Allowable Ranges

A/D Test Voltage	Lower Limit of Allowable Range	Upper Limit of Allowable Range
Internal 0 V	—	7 (VSS_RANGE_MAX)
VDD	0x03F8 (VDD_RANGE_MIN)	—
Internal reference voltage (1.45 V)	0x0113 (VBGR_RANGE_MIN)	0x013A (VBGR_RANGE_MAX)

5.5 List of Functions

Table 5.5 lists the functions that are used in this sample program.

Table 5.5 Functions

Function Name	Outline
R_ADC_Set_TestVoltage	Sets test voltage.
R_ADC_Set_Vss	Sets test voltage to internal 0 V.
R_ADC_Set_Vdd	Sets test voltage to VDD.
R_ADC_Set_Vbgr	Sets test voltage to internal reference voltage.
R_ADC_Set_OperationOn	Enables A/D voltage comparator.
R_ADC_Set_OperationOff	Disables A/D voltage comparator.
R_ADC_Start	Starts A/D conversion.
R_ADC_Stop	Stops A/D conversion.
R_Main_Check_AD_Data	Checks A/D conversion results.
R_ADC_Get_Result	Gets A/D conversion results.
R_Main_Blink_Led	Blinks LED.

5.6 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name]] R_ADC_Set_TestVoltage

Synopsis	Sets test voltage.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Set_TestVoltage(uint8_t testVoltageIndex)
Explanation	Selects the voltage to be used for A/D tests.
Arguments	• testVoltageIndex : Voltage to be used for A/D tests (0, 1, or 2) 0: Internal 0V 1: VDD 2: Internal reference voltage (1.45 V)
Return value	None
Remarks	If voltage is set to a value greater than 2, 2 is assumed.

[Function Name] R_ADC_Set_Vss

Synopsis	Sets test voltage to internal 0 V.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Set_Vss(void)
Explanation	Sets the A/D test voltage to internal 0 V.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Set_Vdd

Synopsis	Sets A/D test voltage to VDD.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Set_Vdd(void)
Explanation	Sets the A/D test voltage to VDD.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Set_Vbgr

Synopsis	Sets A/D test voltage to internal reference voltage.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Set_Vbgr(void)
Explanation	Sets the A/D test voltage to internal reference voltage (1.45 V).
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Set_OperationOn

Synopsis	Enables A/D voltage comparator.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Set_OperationOn(void)
Explanation	Enables the A/D voltage comparator.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Set_OperationOff

Synopsis	Disables A/D voltage comparator.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Set_OperationOff(void)
Explanation	Disables the A/D voltage comparator.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Start

Synopsis	Starts A/D conversion.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Start(void)
Explanation	Enables A/D conversion end interrupts and starts A/D conversion.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Stop

Synopsis	Stops A/D conversion.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Stop(void)
Explanation	Disables A/D conversion end interrupts and stops A/D conversion.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_Main_Check_AD_Data

Synopsis	Checks A/D conversion results.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	uint8_t R_ADC_Check_AD_Data (uint8_t testVoltageIndex)
Explanation	Returns the A/D conversion results.
Arguments	● testVoltageIndex : Voltage to be used for the A/D test (0, 1, or 2) 0: Internal 0 V 1: VDD 2: Internal reference voltage (1.45 V)
Return value	● When the A/D conversion results are within the allowable range: 0x00 ● When the A/D conversion results are outside the allowable range: 0x01
Remarks	If voltage is set to a value greater than 2, 2 is assumed.

[Function Name] R_ADC_Get_Result

Synopsis	Gets A/D conversion results.
Header	r_cg_macrodriver.h r_cg_adc.h r_cg_userdefine.h
Declaration	void R_ADC_Get_Result(uint16_t * const buffer)
Explanation	Shifts the A/D conversion results six bits to the right and places the results in the area specified in the argument.
Arguments	● buffer : Address of the area for storing the A/D conversion results
Return value	None
Remarks	None

[Function Name] R_Main_Blink_Led

Synopsis	Blinks LED.
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_adc.h
Declaration	void R_Main_Blink_Led(void)
Explanation	Blinks LED at intervals of one second. This function forms an infinite loop and control will never be returned to the calling function.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

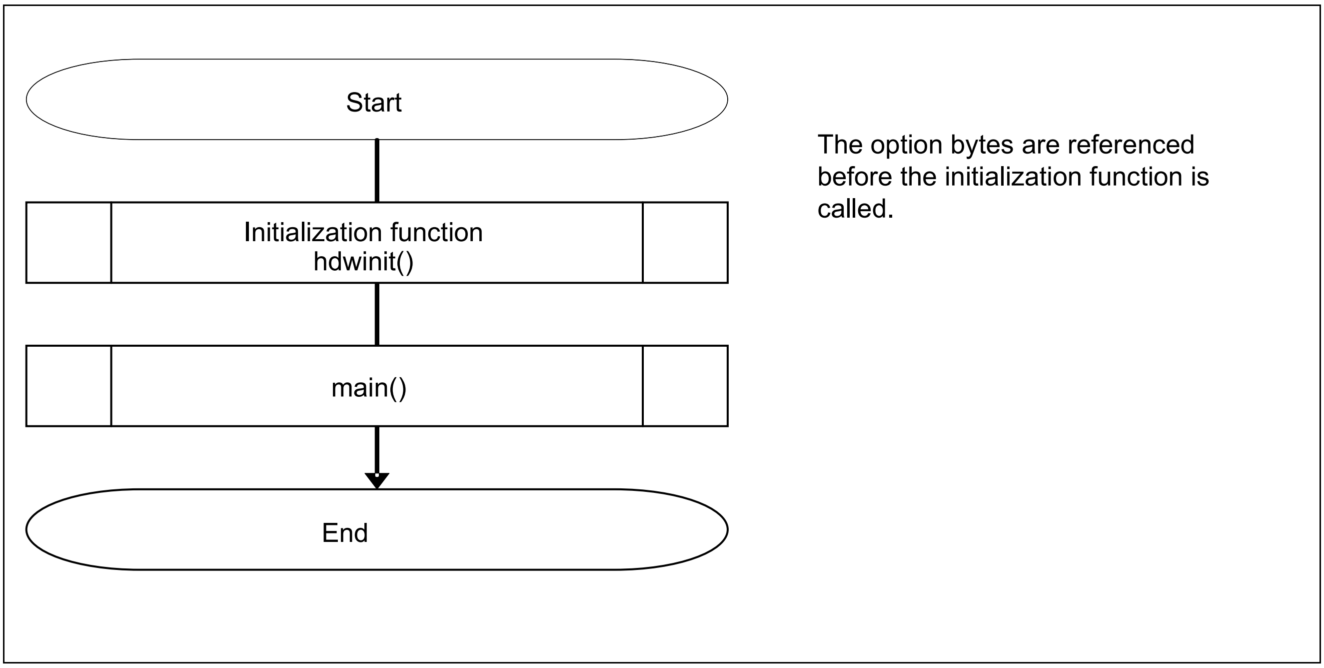


Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

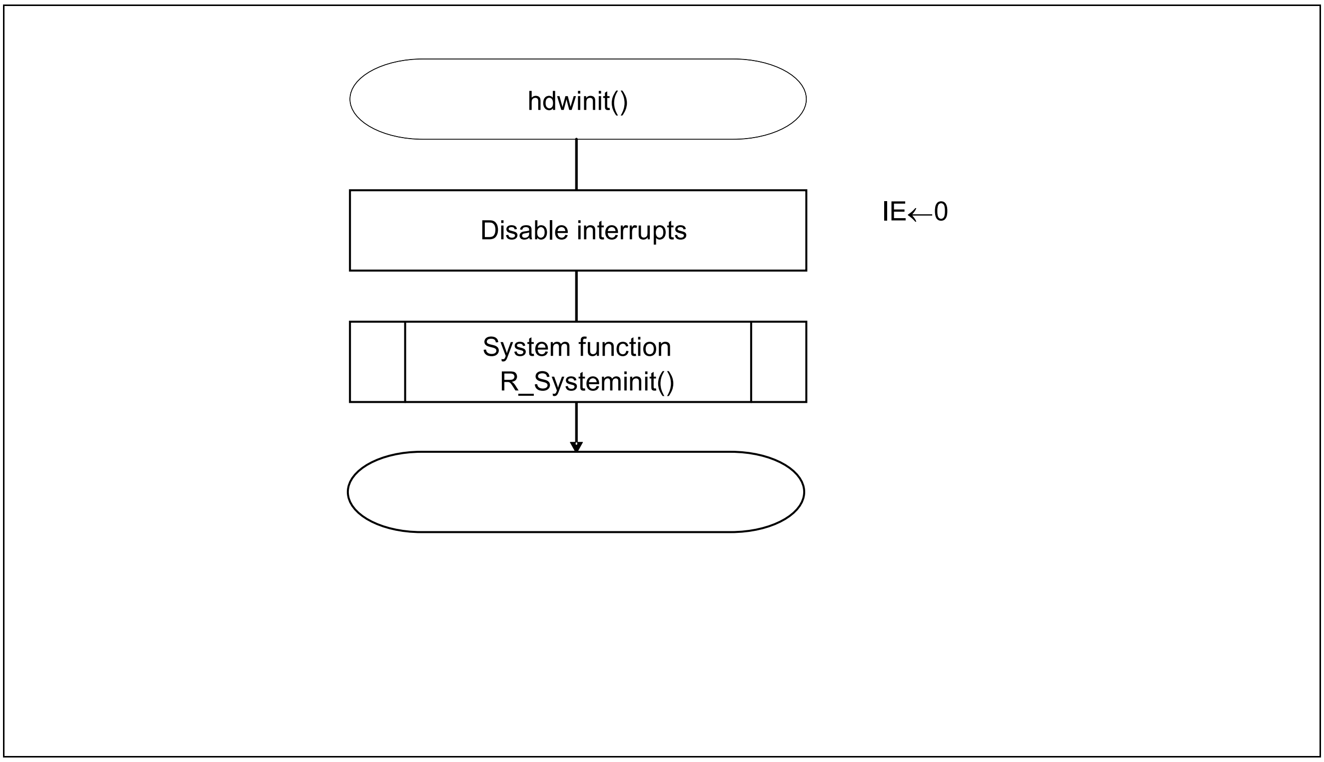


Figure 5.2 Initialization Function

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

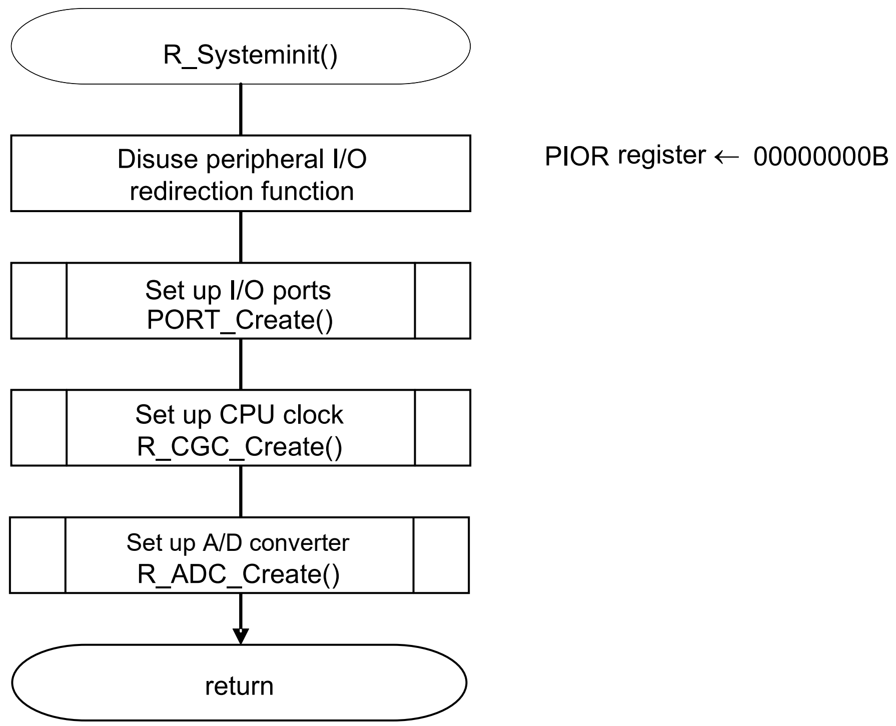


Figure 5.3 System Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

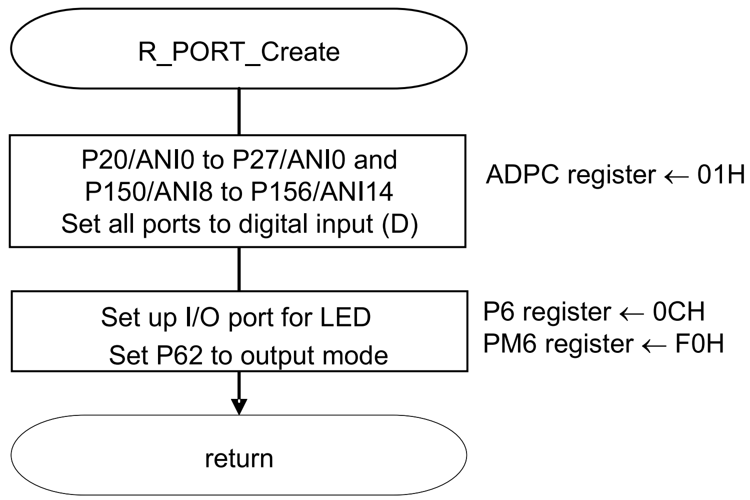


Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the channel to be used for A/D conversion

- A/D port configuration register (ADPC)
  Switches between A/D converter analog input and port digital I/O.

Symbol: ADPC

7	6	5	4	3	2	1	0
0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0
0	0	0	0	**0**	**0**	**0**	**1**

Bits 3 to 0

ADPC3	ADPC2	ADPC1	ADPC0	Available Analog Input
0	0	0	0	ANI0 to ANI14
0	**0**	**0**	**1**	**None**
0	0	1	0	ANI0
0	0	1	1	ANI0 to ANI1
0	0	0	0	ANI0 to ANI2
0	0	0	1	ANI0 to ANI3
0	0	1	0	ANI0 to ANI4
0	0	1	1	ANI0 to ANI5
0	1	0	0	ANI0 to ANI6
0	1	0	1	ANI0 to ANI7
Other than above				Setting prohibited

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

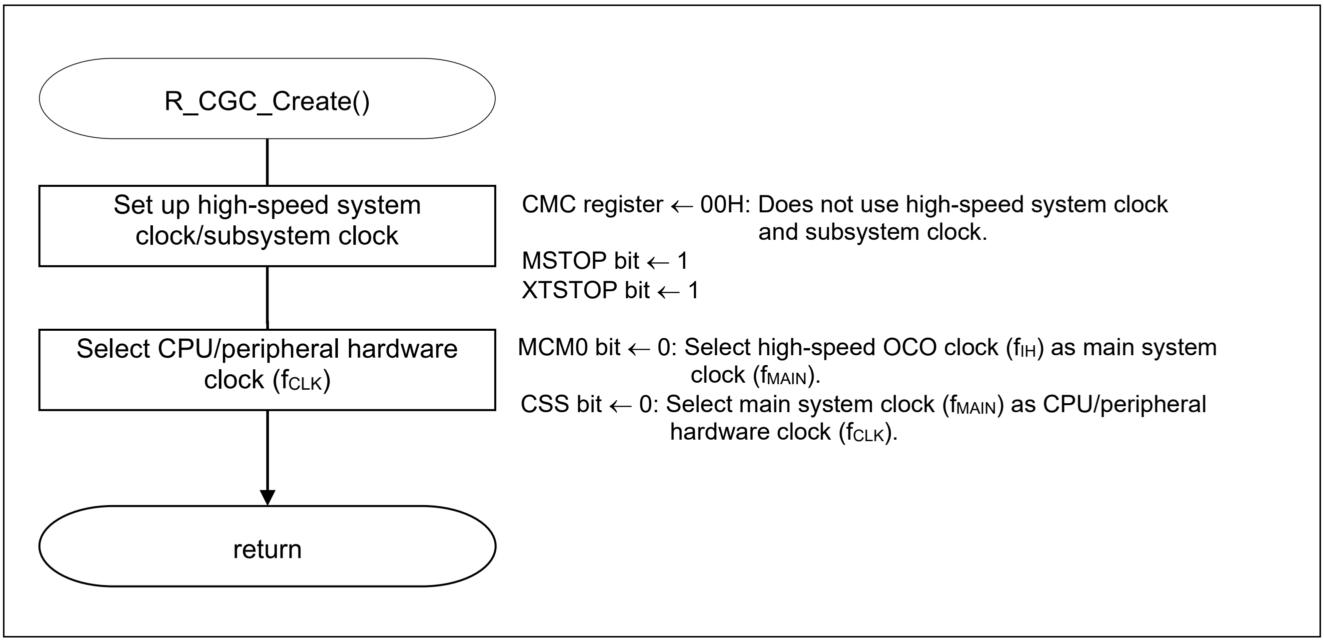


Figure 5.5 CPU Clock Setup

Note: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 Setting up the A/D Converter

Figure 5.6 shows the flowchart for setting up the A/D converter.

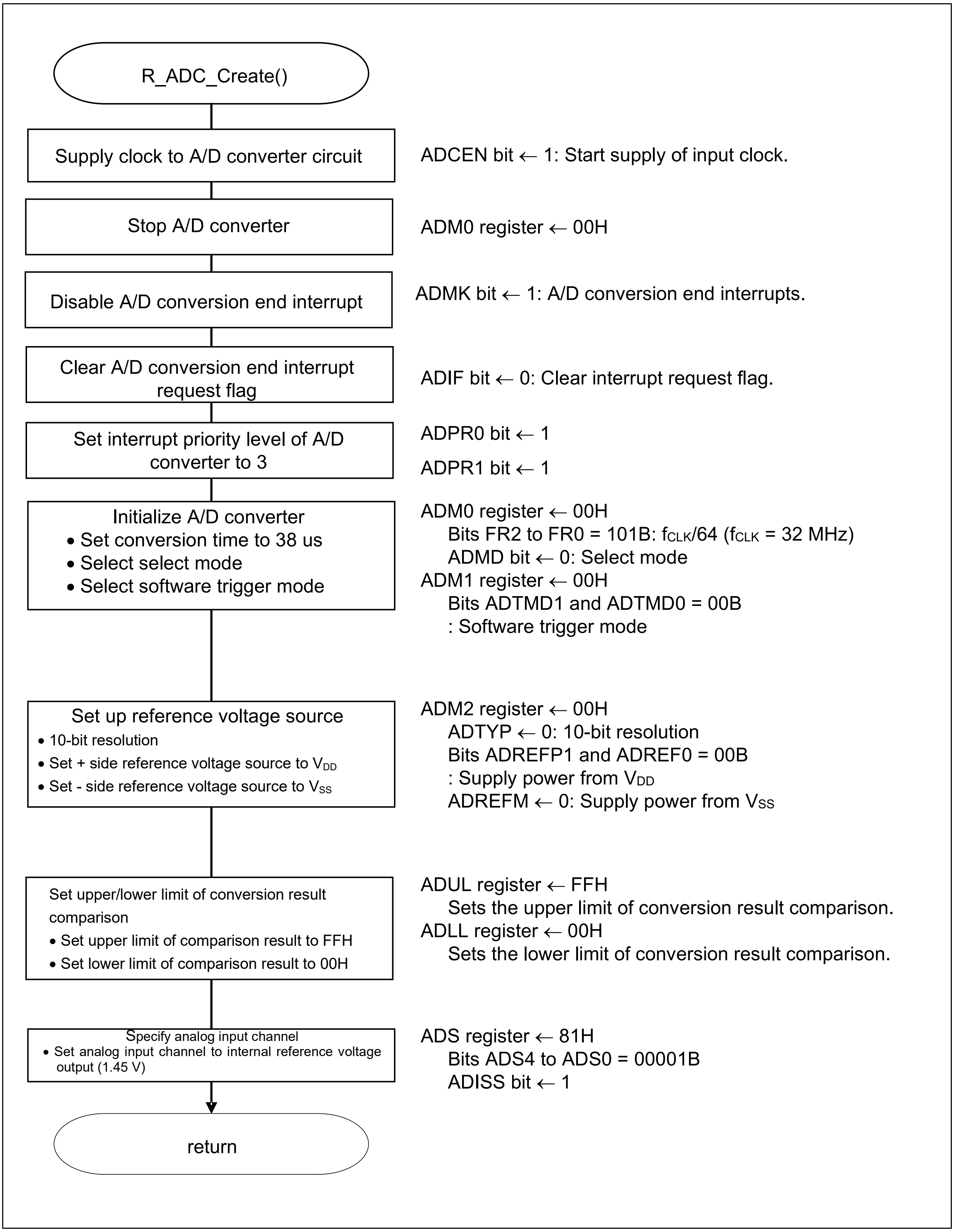


Figure 5.6 A/D Converter Setup

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	0	**1**	x	x	x	0	x

Bit 5

ADCEN	A/D converter input clock control
0	Stops supply of input clock.
1	**Starts supply of input clock.**

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion time and operating mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation**
1	Enables conversion operation

Bit 6

ADMD	A/D channel selection mode select
0	**Select mode**
1	Scan mode

Bits 5 to 1

ADM0					Mode	Conversion Time Selection					Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = **32 MHz**	
0	**0**	**0**	**0**	**0**	**Normal 1**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	**38 µs**	**f_{CLK}/64**
0	0	1							38 µs	19 µs	f_{CLK}/32
0	1	0						38 µs	19 µs	9.5 µs	f_{CLK}/16
0	1	1					38 µs	19 µs	9.5 µs	4.75 µs	f_{CLK}/8
1	0	0					28.5 µs	14.25 µs	7.125 µs	3.5625 µs	f_{CLK}/6
1	0	1					23.75 µs	11.875 µs	5.938 µs	2.9688 µs	f_{CLK}/5
1	1	0					19 µs	9.5 µs	4.75 µs	2.375 µs	f_{CLK}/4
1	1	1				38 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	34 µs	f_{CLK}/64
0	0	1							34 µs	17 µs	f_{CLK}/32
0	1	0						34 µs	17 µs	8.5 µs	f_{CLK}/16
0	1	1					34 µs	17 µs	8.5 µs	4.25 µs	f_{CLK}/8
1	0	0					25.5 µs	12.75 µs	6.375 µs	3.1875 µs	f_{CLK}/6
1	0	1					21.25 µs	10.625 µs	5.3125 µs	2.6536 µs	f_{CLK}/5
1	1	0					17 µs	8.5 µs	4.25 µs	2.125 µs	f_{CLK}/4
1	1	1				34 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	f_{CLK}/2
x	x	x	1	0	Low-voltage 1	Setting prohibited					—
x	x	x	1	1	Low-voltage 1	Setting prohibited					—

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D voltage comparator operation**
1	Enables A/D voltage comparator operation

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion trigger mode

A/D converter mode register 1 (ADM1)
Selects the A/D conversion trigger mode.
Selects the A/D conversion operating mode.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	**0**	**0**	0	0	0	**0**	**0**

Bits 7 and 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	—	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of the A/D conversion mode
0	**Sequential conversion mode**
1	One-shot conversion mode

Bits 1 and 0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	**0**	**Do not use hardware trigger.**
0	1	End of timer channel 1 count or capture interrupt signal (INTTM01)
1	0	Real-time clock interrupt signal (INTRTC)
1	1	Interval timer interrupt signal (INTIT)

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the reference voltage

- A/D converter mode register 2 (ADM2)
  Sets up the reference voltage source.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADCRK	AWC	0	ADTYP
0	**0**	**0**	0	**0**	**0**	0	**0**

Bits 7 and 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.44 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the - side reference voltage source of the A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADCRK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when ADLL register ≤ ADCR register ≤ ADUL register.**
1	The interrupt signal (INTAD) is output when ADCR register < ADLL register and ADUL register < ADCR register.

Bit 2

AWC	Specification of the wakeup function (SNOOZE mode)
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the conversion result comparison upper limit/lower limit

- Conversion result comparison upper limit value register (ADUL)
- Conversion result comparison lower limit value register (ADLL)
  Sets up the upper and lower limits of conversion result comparison.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Specifying the input channel

- Analog input channel register (ADS)
  Specifies the input channel for the analog signal to be subjected to A/D conversion.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
1	0	0	**0**	**0**	**0**	**0**	**1**

Bits 7 and 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog Input Channel	Input Source
0	0	0	0	0	0	ANI0	P20/ANI0 pin/AV_{REFP} pin
0	0	0	0	0	1	ANI1	P21/ANI1 pin /AV_{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	0	1	1	1	ANI7	P27/ANI7 pin
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P147/ANI18 pin
0	1	0	0	1	1	ANI19	P120/ANI19 pin
1	0	0	0	0	0	—	Temperature sensor 0 output
1	**0**	**0**	**0**	**0**	**1**	—	**Internal reference voltage output (1.44 V)**
Other than above						Setting prohibited	

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up A/D conversion end interrupts

- Interrupt request flag register (IF1H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disables interrupts.

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITIMK	RTCMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt processing control
0	Enables interrupt processing.
1	**Disables interrupt processing.**

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 Main Processing

Figure 5.7 and Figure 5.8 show the flowchart for the main processing.

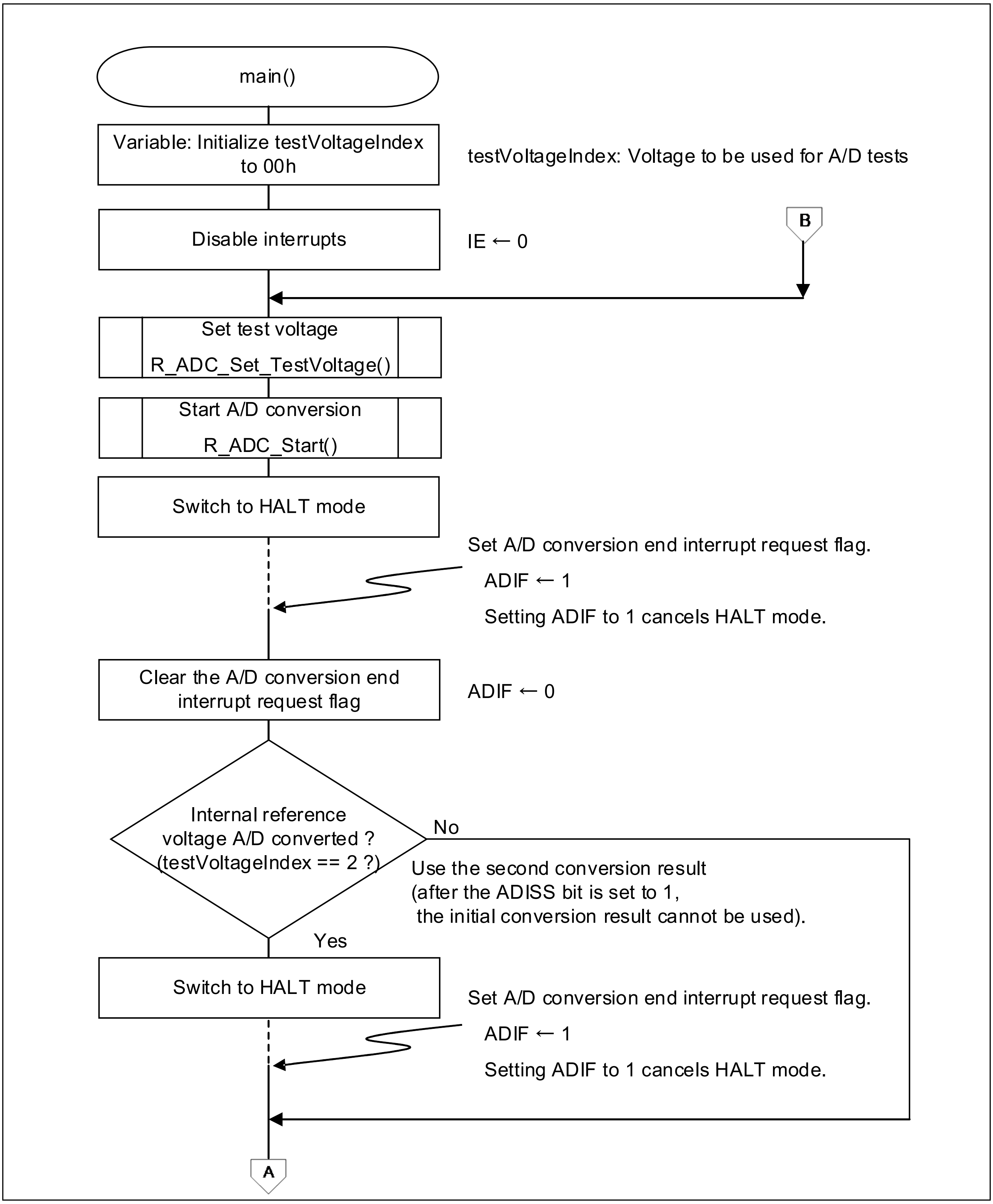


Figure 5.7 Main Processing (1/2)

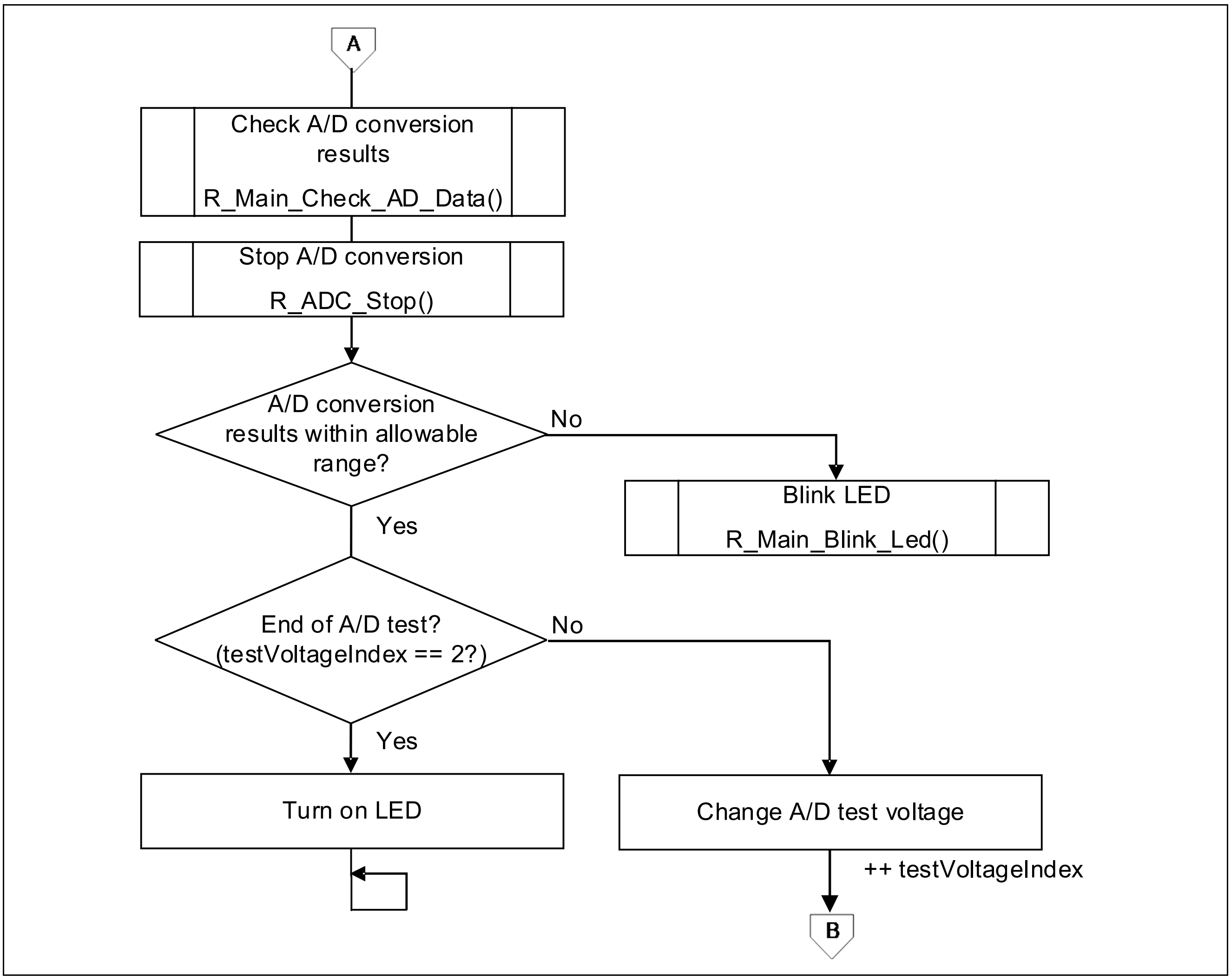


Figure 5.8 Main Processing (2/2)

5.7.7 Setting the Test Voltage

Figure 5.9 shows the flowchart for setting the test voltage.

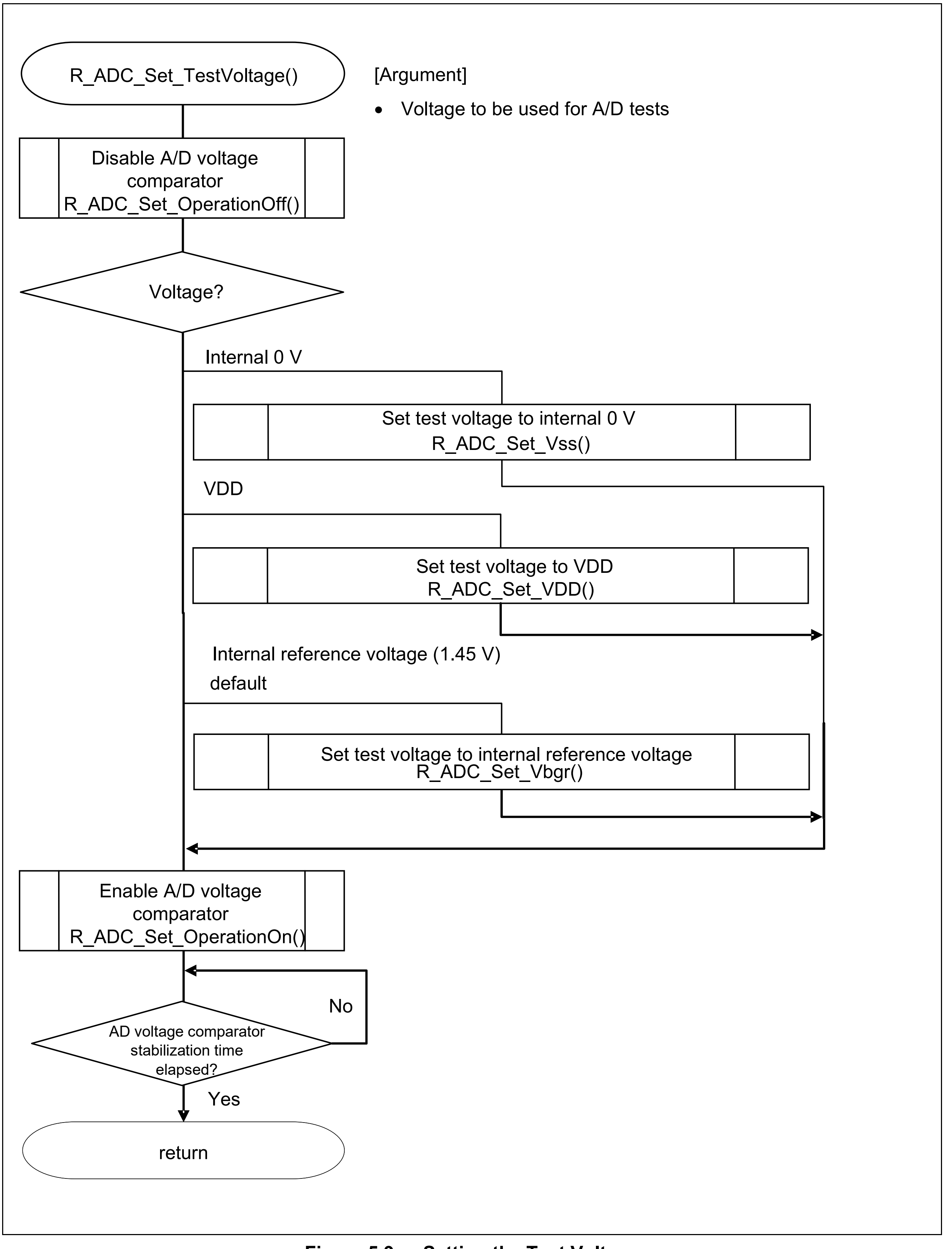


Figure 5.9 Setting the Test Voltage

5.7.8 Setting the Test Voltage to Internal 0 V

Figure 5.10 shows the flowchart for setting the test voltage to internal 0 V.

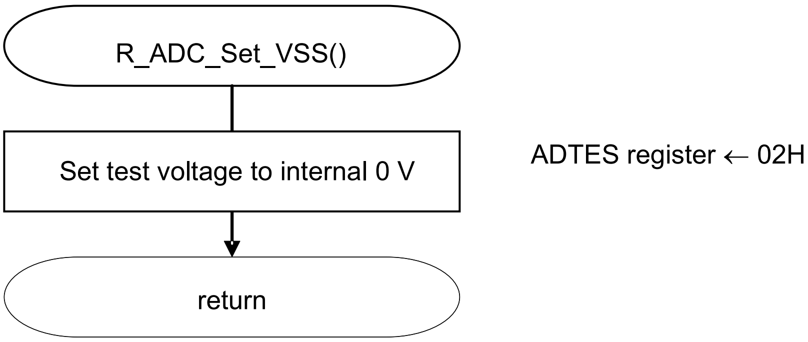


Figure 5.10 Setting the Test Voltage to Internal 0 V

Setting the A/D conversion target

- Set the A/D conversion target.

Symbol: ADTES

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ADTES1	ADTES0
0	0	0	0	0	0	**1**	**0**

Bits 1 and 0

ADTES1	ADTES0	A/D conversion target
0	0	ANIxx (This is specified using the analog input channel specification register (ADS).)
1	**0**	**AV_{RFFM}**
1	1	AV_{RFFP}

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.9 Setting the Test Voltage to VDD

Figure 5.11 shows the flowchart for setting the test voltage to VDD.

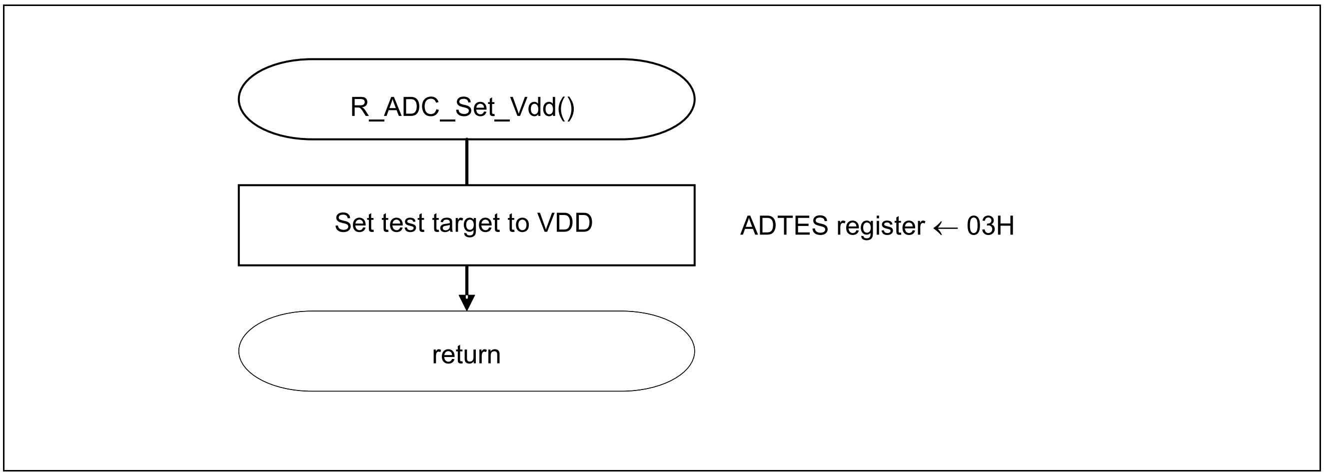


Figure 5.11 Setting the Test Voltage to VDD

Setting the A/D conversion target

- Sets the A/D conversion target.

Symbol: ADTES

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ADTES1	ADTES0
0	0	0	0	0	0	**1**	**1**

Bits 1 and 0

ADTES1	ADTES0	A/D conversion target
0	0	ANIxx (This is specified using the analog input channel specification register (ADS).)
1	0	AV_{RFFM}
1	**1**	**AV_{RFFP}**

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.10 Setting the Test Voltage to Internal Reference Voltage

Figure 5.12 shows the flowchart for setting the test voltage to internal reference voltage.

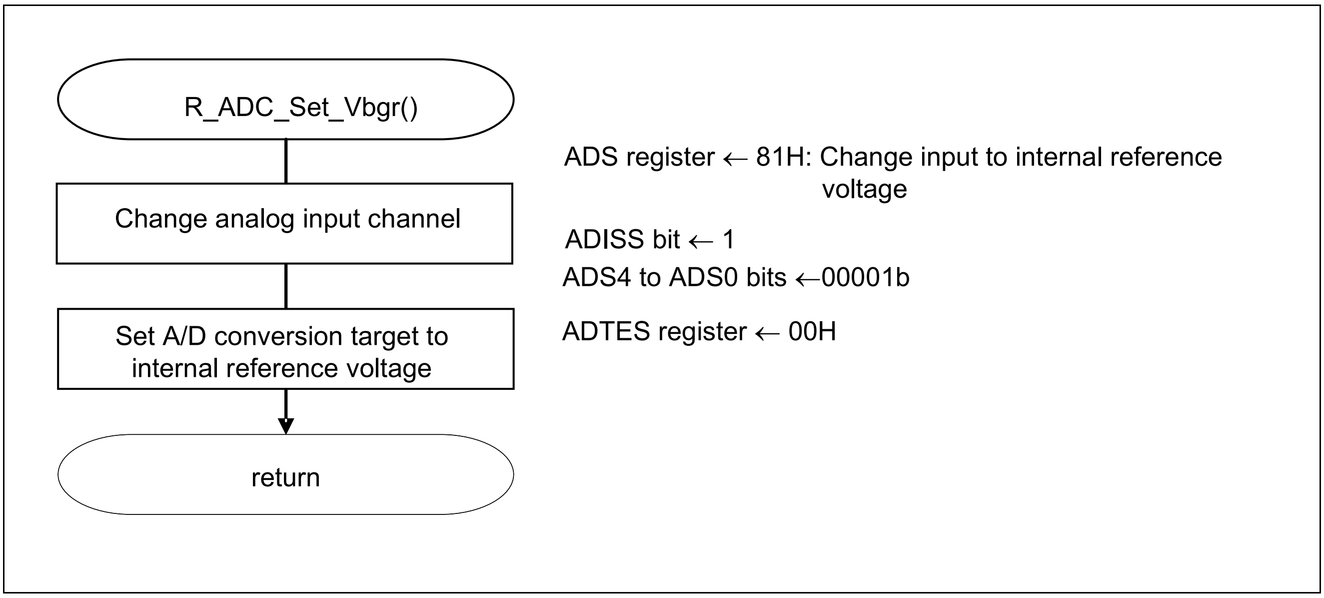


Figure 5.12 Setting The Test Voltage to Internal Reference Voltage

Setting the A/D conversion target

- Set the A/D conversion target.

Symbol: ADTES

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ADTES1	ADTES0
0	0	0	0	0	0	**0**	**0**

Bits 1 and 0

ADTES1	ADTES0	A/D conversion target
0	**0**	**ANIxx (This is specified using the analog input channel specification register (ADS).)**
1	0	AV_{RFFM}
1	1	AV_{RFFP}

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.11 Enabling the A/D Voltage Comparator

Figure 5.13 shows the flowchart for enabling the A/D voltage comparator.

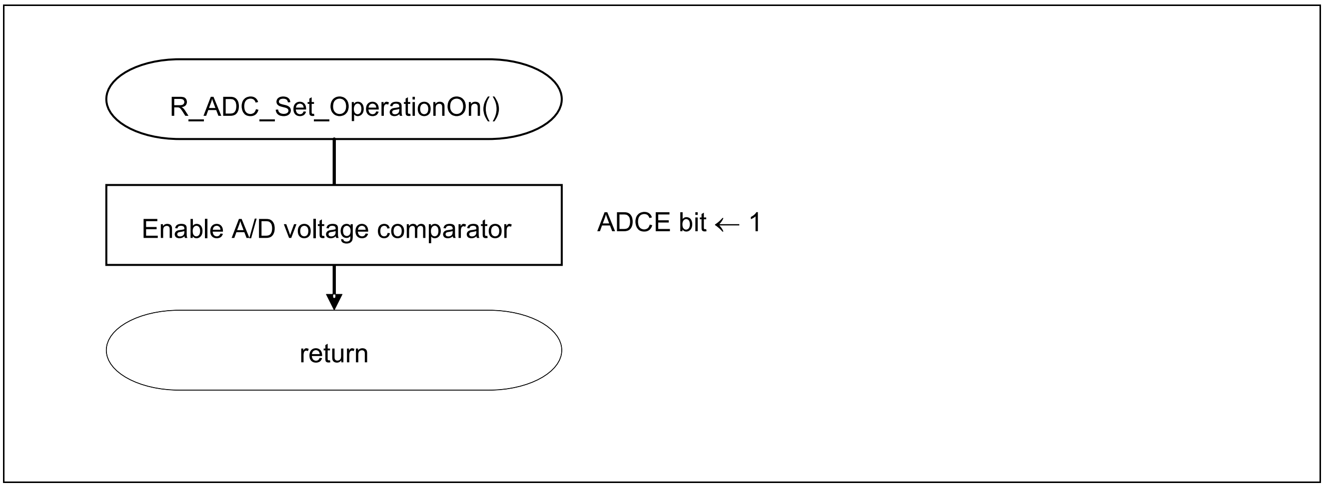


Figure 5.13 Enabling the A/D Voltage Comparator

Starting the A/D voltage comparator

- A/D converter mode register 0 (ADM0)
  Controls the operation of the A/D voltage comparator.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	x	x	x	x	x	x	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	**Starts A/D voltage comparator operation**

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.12 Disabling the A/D Voltage Comparator

Figure 5.14 shows the flowchart for disabling the A/D voltage comparator.

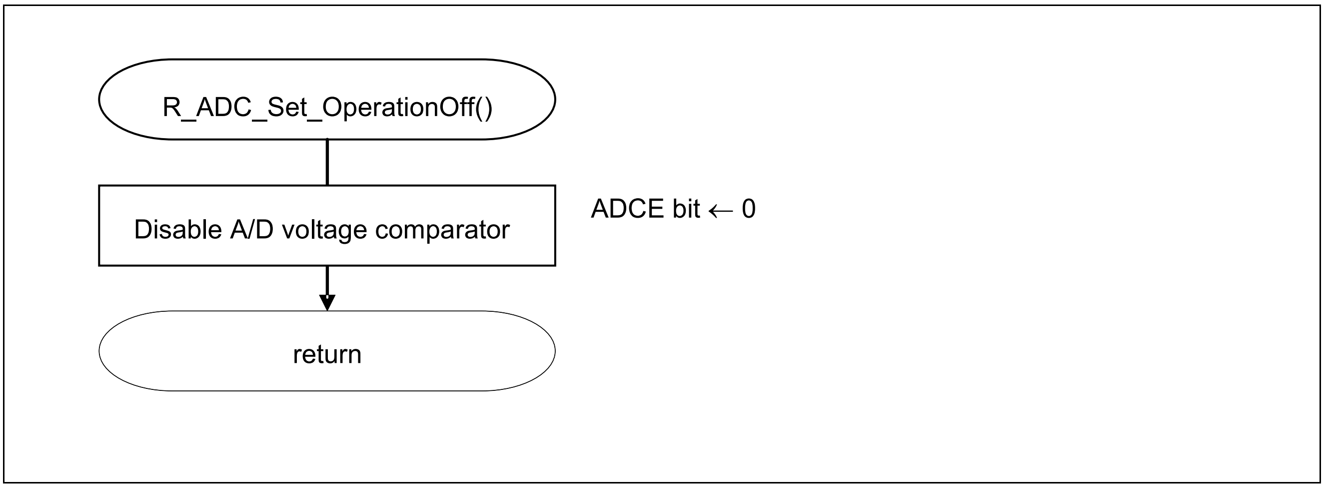
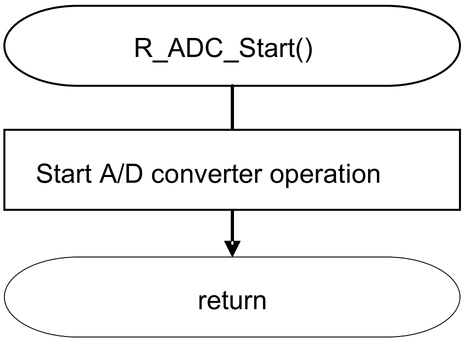


Figure 5.14 Enabling the A/D Voltage Comparator

5.7.13 Starting A/D Conversion

Figure 5.15 shows the flowchart for starting A/D conversion.



ADIF bit ← 0: Clear interrupt request flag.
ADMK bit ← 0: Enable end of A/D conversion interrupt processing.
ADCS bit ← 1: Enable conversion operation.

Figure 5.15 Starting A/D Conversion

Starting conversion operation

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV2	ADCE
1	x	x	x	x	x	x	1

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation
1	**Starts conversion operation**

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.14 Stopping A/D Conversion

Figure 5.16 shows the flowchart for stopping A/D conversion.

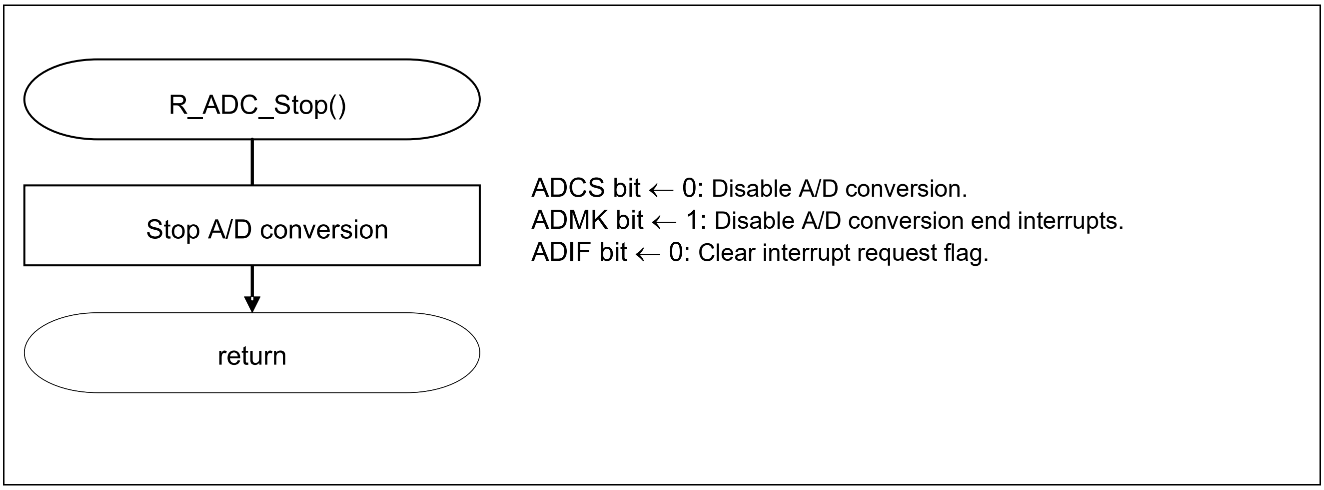


Figure 5.16 Stopping A/D Conversion

5.7.15 Checking the A/D Conversion Results

Figure 5.17 shows the flowchart for checking the A/D conversion results.

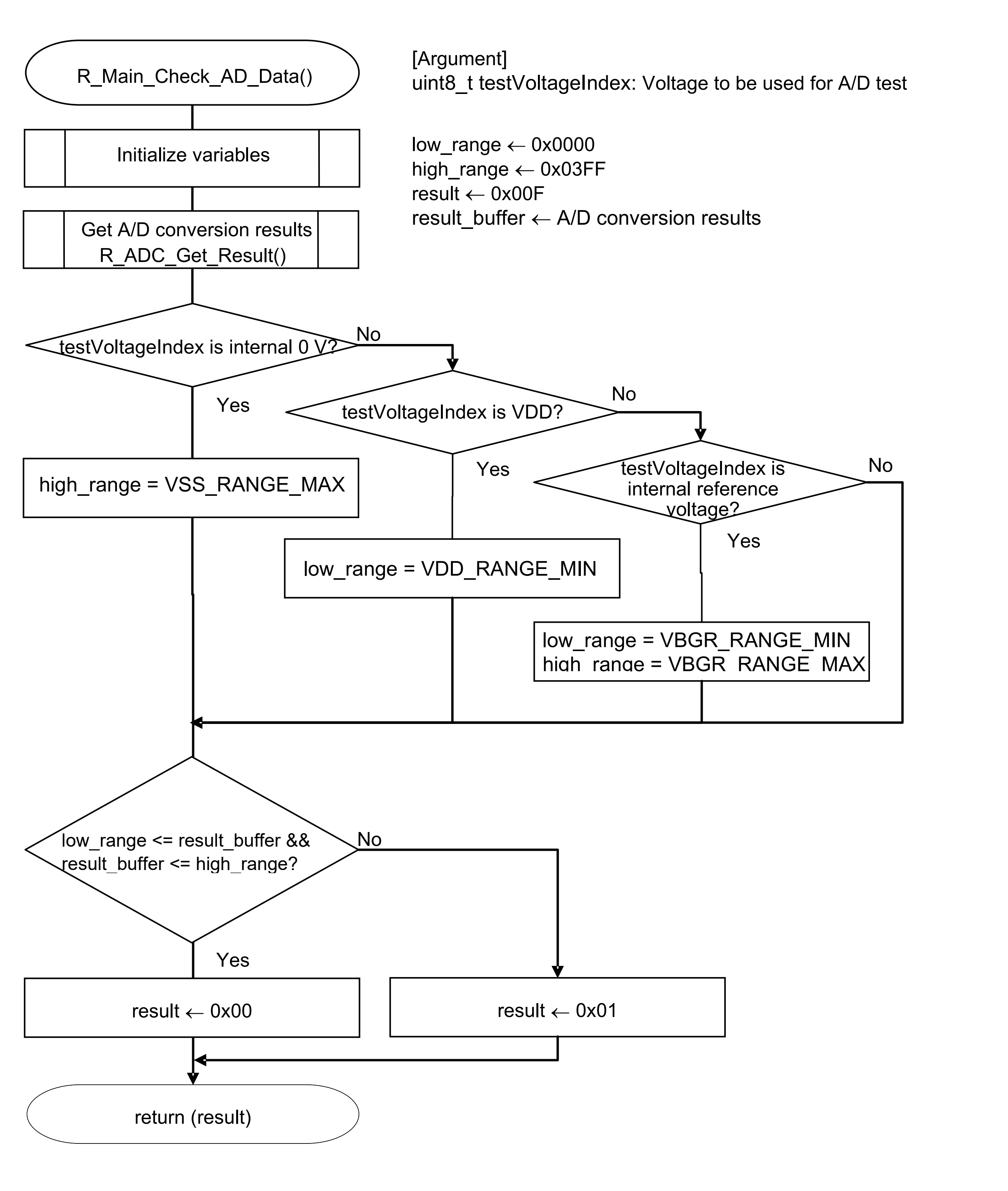


Figure 5.17 Checking the A/D Conversion Results

5.7.16 Getting the A/D Conversion Results

Figure 5.18 shows the flowchart for getting the A/D conversion results.

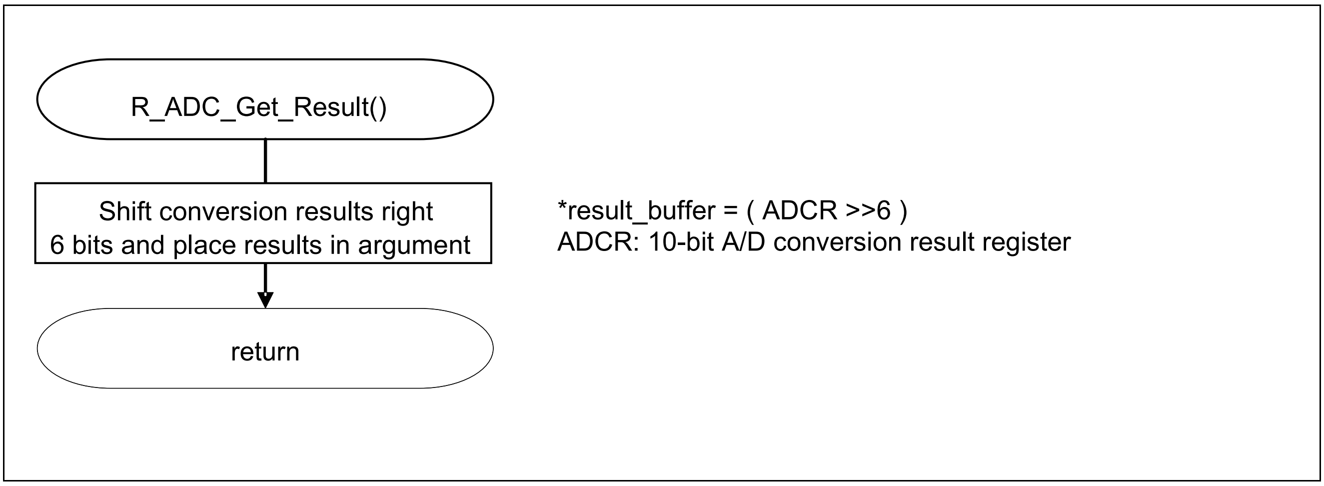


Figure 5.18 Getting the A/D Conversion Results

5.7.17 Blinking the LED

Figure 5.19 shows the flowchart for blinking the LED.

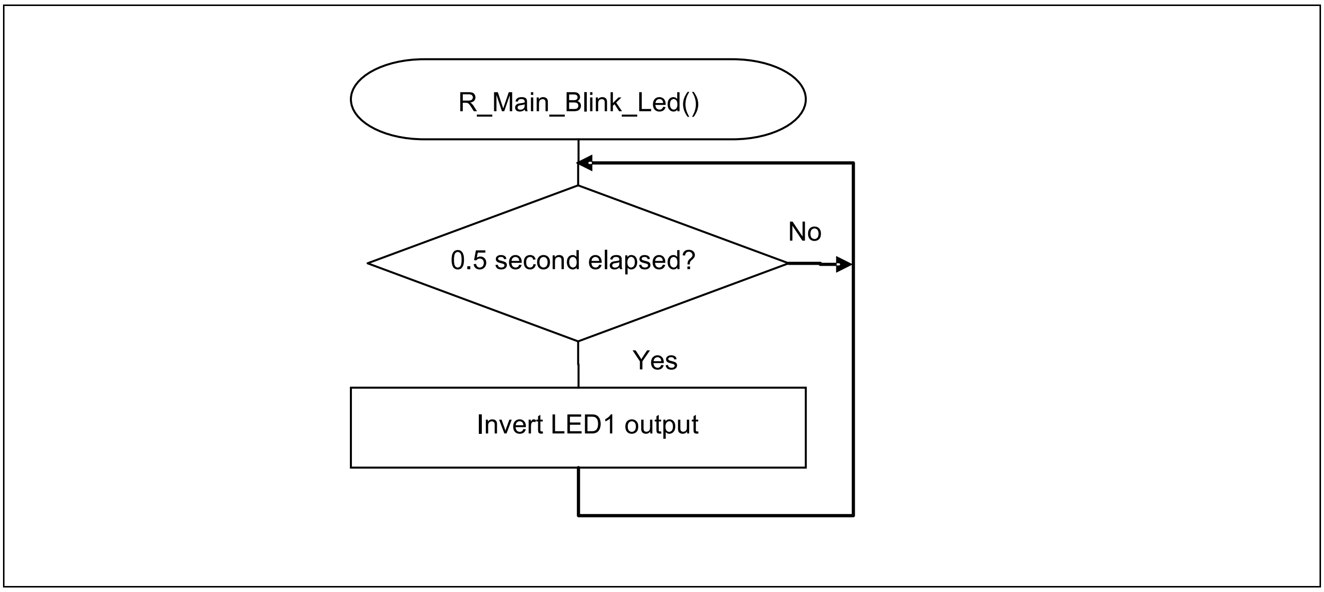


Figure 5.19 Blinking the LED

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Website and Support

Renesas Electronics Website

- http://www.renesas.com/index.jsp

Inquiries

- http://www.renesas.com/contact/

Revision Record	RL78/G13 Safety Function (A/D Test)

Rev.	Date	Description	
		Page	Summary
1.00	May 28, 2015	—	First edition issued
1.01	June.02.21	4 29-30	Updated the Operation Confirmation Conditions. Updated example code.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   1. A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   2. The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   3. Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   4. Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   5. After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   6. Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   7. Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   8. Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   9. "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   10. "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   11. Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

12. For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.